Small Area Phase Correction Circuit for RVDT Using XOR Phase Detector

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Abstract: - In this paper, we propose a signal processing circuit using Phase Locking method for phase correction of RVDT sensor. A digital phase correction method using a conventional demodulator has been used to correct the phase using demodulation signals. Therefore, the chip size increases because a ROM table is needed to generate the demodulation signal. Proposed phase correction circuit is performed using a reference signal instead of a demodulation signal for phase correction. The chip size decreases because there is no need to make a demodulation signal. The design is TSMC 0.18um CMOS technology and the supply voltage is 1.8V. The proposed circuit has a 94% reduction in chip size compared to the conventional Costas loop type circuit.

Key-Words: - Rotary Variable Differential Transformer (RVDT), Sensor, Phase correction, Demodulation, Signal processor, Costas Loop

1 Introduction

In this paper, we propose a signal processing circuit for phase correction of Rotary Variable Differential Transformer (RVDT) sensor. As a car uses more electronic sensors, RVDT can be a good solution for angular sensors with high linearity and high reliability. The RVDT has differential output and good characteristics such as long period reliability, high-resolution and high-linearity. On this basis, it is widely used in industrial application that requires high-resolution and high-linearity [1]. Therefore, a circuit for processing the signal of this sensor is designed.

Here, the design was carried out using the digital phase correction method. A phase correction method using a conventional demodulator requires a ROM table for demodulation signals [2]. Since the sampled input signal is compared with the demodulated signal to perform the phase correction, many ROM table for demodulation signals data and a high sampling frequency of the input signal is required for accurate phase correction. Also, since the RVDT input / output signal and the demodulation signal must be in the same phase, it takes a long time to process in the loop.

The proposed circuit performs phase correction by using the RVDT input signal as the reference signal and the output signal as the modulation signal. Therefore, the area used in the ROM table can be reduced because there is no need to generate a demodulation signal. In addition, since only the phase of the RVDT input / output signal needs to be matched, the phase correction time is expected to be reduced compared with the case of using the demodulator.

In Section 2, we show the problem of the Costas Loop circuit applying the demodulation method. The proposed circuit and the simulation result are described in section 3. The conclusion is shown in section 4.

2 Conventional circuit

Costas Loop is a signal processing circuit that tracks the phase of an input signal by applying a demodulation scheme. The Costas Loop consists of Voltage Controlled Oscillator (VCO), Loop Filter (LF), Phase Detector (PD), Low Pass Filter (LPF) and multiplier. Fig.1 is block diagram of Costas Loop [3]-[5].

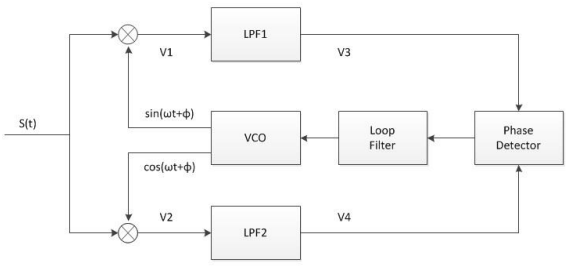

Fig. 1 Block diagram of Costas Loop

The input signal S(t) is a modulated signal as shown in equation (1). φ_1 is the phase difference between the message signal and the carrier signal.

$$S(t) = A(t)\sin(\omega t + \varphi_1) \quad (1)$$

V1 is a signal that is phase-corrected through the loop, and is expressed by Equation (2). V2 is a phase error signal and is expressed as Equation (3).

$$V1 = \frac{1}{2}A(t)\cos(\varphi_1 - \varphi_2) - \frac{1}{2}A(t)\sin(2\omega t + \varphi_1 + \varphi_2) \quad (2)$$

$$V2 = \frac{1}{2}A(t)\sin(\varphi_1 - \varphi_2) + \frac{1}{2}A(t)\sin(2\omega t + \varphi_1 + \varphi_2) \quad (3)$$

The double-frequency component can be removed by passing the signal through a low pass filter. This filtering yields the in-phase component where $\Delta\varphi = \varphi_1 - \varphi_2$ is the phase error.

$$V3 = \frac{1}{2}A(t)\cos(\varphi_1 - \varphi_2) \quad (4)$$

$$V4 = \frac{1}{2}A(t)\sin(\varphi_1 - \varphi_2) \quad (5)$$

Loop filter plays a key role in Costas loop. Its main function is to filter out the high frequency phase detector leakage component. This filter generates the VCO control voltage according to the error from the phase.

When the Costas Loop is trying to achieve the lock state, the output of the loop filter gradually decreases so that the output of the VCO has zero or a constant phase difference to the input signal and has the same frequency as that of the input signal.

In this case, the digital amplitude information corresponding to $1/4$ period of the sine wave is stored in the ROM table. A demodulation signal is generated by the data of the stored ROM table.

The more data of the demodulation signal, the less the phase error. However, as the data of the demodulated signal increases, the size of the ROM table also increases, resulting in an increase in the chip size. If the amount of data is small, it takes a long time to lock when the sampling rate of the modulated signal is low. This is because when the modulated signal is close to 0, the part that matches the demodulated signal data cannot be found and data processing is not performed.

3 Proposed circuit

The proposed circuit removes the demodulation signal and performs phase correction with the RVDT reference signal and the modulated signal.

The phase of the reference signal B of the RVDT and the phase of the modulation signal A of the RVDT are measured and delayed. The circuit is shown in Fig.2.

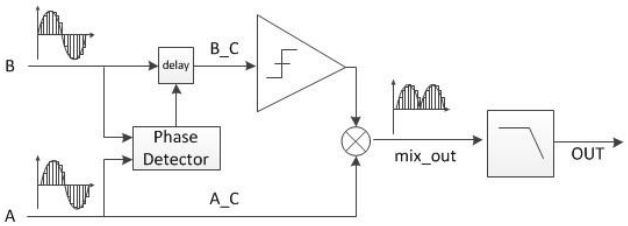

Fig. 2 Block diagram of proposed circuit

The phase detector is configured as shown in Fig.3 and can measure phase difference between 0 and 90 degrees and phase difference between 180 and 270 degrees.

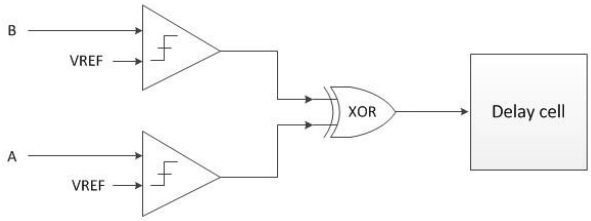

Fig. 3 Phase Detector circuit

The reference signal B and the modulated signal A were made into a square wave using a comparator. The phase difference of the signal was measured by using an XOR gate on two square waves.

The phase of the reference signal B was delayed by counting the difference in the number of samples of the two signals using the phase detector with the reference signal B and the modulated signal A. The waveform is shown as Fig.4.

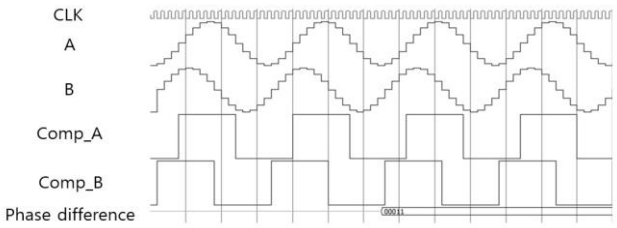

Fig. 4 Wave of Phase Detector circuit

Fig.5 shows the waveforms of the modulated signal A and the phase-corrected reference signal B.

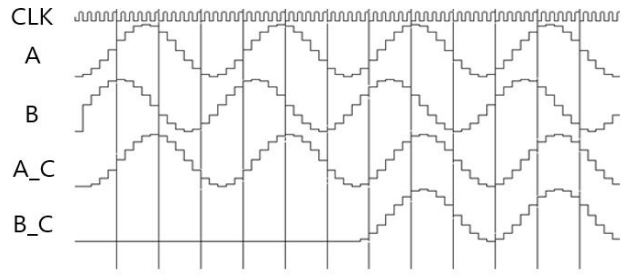

Fig. 5 Wave of Phase shift

The reference signal B is made into a square wave using a comparator and multiplied by the modulation signal A to form a rectified signal. The proposed circuit multiplies the modulated signal A by the reference signal B to find the phase difference of 180 degrees and to process the negative value.

The filter uses a moving average filter and the transfer function is calculated as (6) ~ (9). The filter characteristics are shown in Fig.6 [6][7].

$$H(z) = 1 + z^{-1} + \cdots + z^{-63} \quad (6)$$

$$z^{-1}H(z) = z^{-1} + z^{-2} + \cdots + z^{-64} \quad (7)$$

$$H(z)(1 - z^{-1}) = 1 - z^{-64} \quad (8)$$

$$H(z) = \frac{1-z^{-64}}{1-z^{-1}} \quad (9)$$

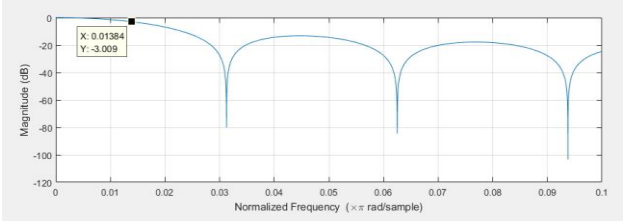

Fig. 6 Frequency characteristic

The DC gain of this filter is 64 and the gain after rectification is calculated as follows.

Here, the gain of the filter is not 1/64. The lower 6 bits of the filter output are used as the decimal point.

$$\text{Gain} = \frac{64}{\pi}\int_0^{\pi} \sin\omega \; d\omega$$

$$= \frac{128}{\pi} \quad (10)$$

Fig.7 shows the input and output waveforms of the system. The waveform A is a modulated signal and the waveform B is the reference signal. The mix_out is a rectifier signal of A and OUT is a phase-corrected message signal using a filter.

Table 1 Simulation specification

CLK[Hz]	2.4M
Message signal Frequency[Hz]	100
Reference signal frequency[Hz]	10K
Sampling late[S/s]	160K
Input resolution[bit]	12

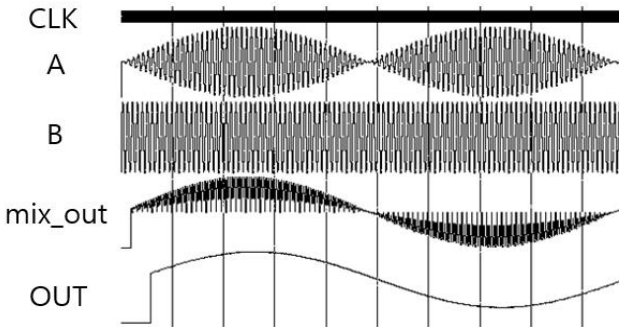

Fig. 7 Waveform of proposed circuit

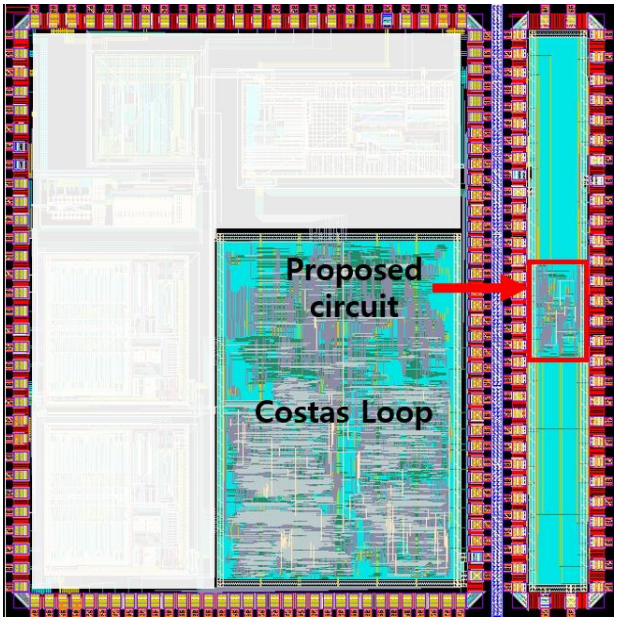

Fig. 8 Layout comparison

The layout size of the Costas Loop is 1872um * 2760um, and the layout size of the proposed circuit is 370um * 760um. The proposed circuit has about 94% smaller area than the existing Costas loop circuit. The layout size comparison is shown as Fig.8.

The chip was fabricated by using TSMC 0.18μm CMOS technology.

4 Conclusion

In this paper, we propose a signal processor circuit using Phase Locking method for phase correction of RVDT sensor and compared it with Costas Loop and designed to reduce the chip size.

Instead of the Costas Loop method using the conventional demodulator, the phase is corrected using the input / output signal of the RVDT sensor. Accordingly, the ROM table for the demodulation signal is removed and the number of filters is reduced from three to one.

As a result, the size of the chip was reduced by about 94% from 1872um * 2760um to 370um * 760um. It is also expected that the processing time will be reduced because the process steps have been reduced.

Acknowledgment

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References:

[1] Jong-Kyoung Lee, Young-Hun Ko, Sang-Gug Lee, Calibration Technique for Sensitivity Variation in RVDT Type Accelerator Position Sensor, *2013 IEEE International Instrumentation and Measurement Technology Conference (I2MTC)*, 2013, pp. 1512-1516

[2] B. Shamla, K. G Gayathri Devi, Design and Implementation of Costas loop for BPSK Demodulator, *2012 Annual IEEE India Conference (INDICON)*, 2012, pp. 785-789

[3] Yan Dangui, Tong Ruijun, Xiong Min, Zhang Chengchang, An optimal method for Costas Loop design based on FPGA, *2013 Fourth International Conference on Digital Manufacturing & Automation*, 2013, pp. 175-179.

[4] Huimei Yuan, Xiaoguang Hu, Juyong Huang, Design and Implementation of Costas Loop Based on FPGA, *2008 3rd IEEE Conference on Industrial Electronics and Applications*, 2008, pp. 2383-2388.

[5] Rodger E. Ziemer, William H. Tranter, *Principles of Communications Systems, Modulation, and Noise sixth edition*, John Wiley & Sons, 2008.

[6] John G. Proakis, Dimitris G. Manolakis, *Digital Signal Processing Principles, Algorithms, and Applications third edition*, Prentice-Hall International, 1996.

[7] Lakshmanan S. A., Amit Jain, B. S. Rajpourhit, Analysis and Design of Adaptive Moving Average Filters based Low-Gain PLL for Grid Connected Solar Power Converters, *2015 IEEE Power & Energy Society General Meeting*, 2015, pp. 1-5