RHBD Charge Pump PLL based 2.4 GHz Frequency Synthesizer

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Abstract: Frequency Synthesizer forms the heart of electronic communication system. Phase Locked Loop (PLL) based Frequency Synthesizers over the years has become the ubiquitous solution for generation of stable clock source. But it is a challenging task to design and develop PLL to be used in radiation environment such as in satellites, space systems and military electronics. Since impact of radiation strike on PLL is said to introduce transient faults resulting in increased timing jitter, distortion in phase, and bit flips. One or more of the above said effects can initiate false triggering which may result in incorrect data to be latched, loss of synchronization in data processing and networking. This may lead to catastrophic effect. Hence, as the stability of frequency synthesizer is of vital importance, there is a stressful need for design of radiation hard, fault tolerant frequency synthesizer. With this motivation, in this paper, a radiation hard CMOS Charge Pump PLL is designed to synthesize a 2.4GHz frequency source using 20MHz reference input frequency. The proposed radiation hard PLL design uses a hybrid Radiation Hardening By Design (RHBD) fault tolerant technique combined with redundancy, hence offering a twofold level of fortification from radiation spikes. Cadence tool was used for simulation. The PLL designed has exhibited satisfactory performance. The RHBD Charge Pump PLL in presence of radiation strike resulted in rms jitter of 128.9ps, phase noise of -94.03dbc/Hz and settling time of 159ns against the IEEE 802.11b/g standard requirement of 250ps jitter, -110dbc/Hz phase noise and 10us setting time.

Keywords: SET, Charge Pump PLL, Jitter, Phase Noise, Frequency Synthesis, SEE, TID Radiation Tolerant, RHBD, Ring VCO

1. Introduction

PLLs are used in many time critical applications such as frequency synthesis, clock recovery, data recovery and are mainly used as frequency source generators in space bound communication systems [1]. The basic objective of the PLL used in these applications is to generate an output frequency source which is in phase with the input reference frequency signal. PLL based frequency synthesizer circuits being the heart of any space bound electronic system have been identified as single event soft point as they are highly sensitive to radiation spikes. Their reliable operation is critical for the accurate performance of systems operating in radiation environments.

Transient faults introduced in PLL due to radiation strike results in increased timing jitter, distortion in phase, and bit flips. This can initiate false triggering which may result in incorrect data to be latched, loss of synchronization in data processing and networking [2]. Loss in synchronisation introduces instability or unexpected behaviour resulting in malfunction of the system or even catastrophic failure. Thus it is of paramount significance to design Radiation Tolerant PLL.

This paper gives an overview of Charge Pump PLL (CP-PLL) operation, effect of radiation on CP-PLL, radiation hardening mechanisms and design of a Radiation Tolerant CP-PLL using

Radiation Hard by Design (RHBD) approach. In the following section we discuss the working of Integer N Charge Pump PLL based frequency synthesizer.

2. Frequency Synthesizer Operation

A typical Integer N type Charge Pump PLL as shown in Figure 1, consists of a Phase Frequency Detector (PFD), a Charge Pump (CP), a Loop Filter (LPF), a Voltage Controlled Oscillator (VCO) and a Divider.

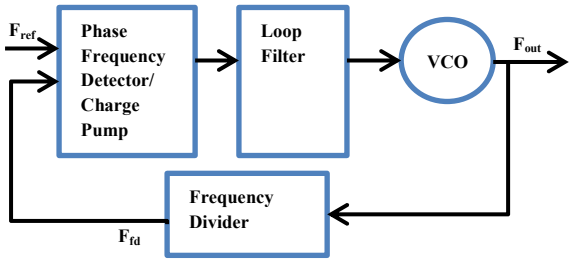

Fig 1. Block Diagram of Integer N Charge Pump PLL based Frequency Synthesizer.

The output of the VCO is divided in frequency by a frequency divider by a factor „N" and is compared with the reference clock in the PFD, where the reference frequency and the feedback frequency phases are compared, to generate an error signal. The charge pump then converts the error signal into analog current, which are averaged over time and converted to a voltage value by the passive loop filter. This control voltage drives the VCO to generate a specific frequency clock. Hence phase difference will be detected and the charge-pump will adjust the control voltage until the phase difference between the reference clock and the divided VCO clock is zero, the VCO will run at exactly N times the frequency of the reference clock.

$$f_{out} = N * f_{ref} \quad (1)$$

Normally a low frequency stable crystal oscillator is used as a reference oscillator. By choosing the divider ratio „N" appropriately, the synthesizer generates an output of the desired frequency that inherits much of the stability of the input reference oscillator, making PLL a low cost, vital component for generation of high frequency clock source.

3. Effect of Radiation on PLL

Radiation effect on PLL can be categorized into Total Ionization Dose effect (TID) and Single Event Effect (SEE). The cumulative effect caused primarily by abundant energetic particles over a long period of time is called as TID effect. TID may drift the threshold voltages or increase leakage currents in voltage controlled oscillators (VCO), which could eventually cause the PLL to malfunction. However with technology scaling TID effect can be mitigated. In contrast, SEE resulting from a single high energetic particle such as heavy ions penetrating a semiconductor material, can change the logic state of digital circuits. SEE effects the logic states of frequency dividers and phase/frequency detectors in the ADPLL resulting in change at the output synthesized frequency. Also, an "SEE hit" might change the voltage level at the output of charge-pump or loop filter of PLL. This would lead to erroneous output for a certain period of time or the PLL completely goes out of lock.

4. Radiation Hardening

Radiation hardening is a process of making electronic components and systems resistant to damage or malfunction caused by ionizing radiation. Ionizing radiation can be particle radiation and high energy electromagnetic radiation. Ionizing radiation is present in outer space, in high altitude flight, around nuclear reactors and particle accelerators [3].

Radiation Hardening can be realized through design or manufacturing process variations to reduce susceptibility to radiation damage. Radiation hardening

techniques are focused on two methods namely:
1 Radiation Hardening by Process (RHBP)
2 Radiation Hardening by Design (RHBD)

A Previous Related Works

Radiation Hardening by Process: Over the last thirty years, the preferred method for fabricating radiation hardened parts has been by using boutique, dedicated foundries with specialized processes. The approach is often referred to as hardening-by-process [3]. RHBP achieves radiation hardening via process modifications. It is the traditional approach used by radhard foundries. RHBP by process includes the use of Silicon Germanium (SiGe), Silicon on Sapphire (SOS) and Silicon on Insulator (SOI) process. Gosh [4] proposed an approach for designing a radiation hard PLL using SOS-CMOS process. Radiation hardness is achieved through improving circuit design by using a fully self-bias architecture. However a monolithic crystal wafer of sapphire is about twice as expensive to fabricate as a silicon wafer and the LC VCO used do not have good tuning range. Literature survey is made on radiation hard PLLs using SOS CMOS process [5-7]. Matsuura et.al [8] designed a phase-locked loop (PLL) operating at 200 MHz using 0.2 μm fully depleted silicon-on-insulator (SOI) technology. Chen et al. [9] designed a radiation-hardened low-jitter PLL with a low-mismatch charge pump and a robust voltage-controlled oscillator in a 130 nm PD-SOI process. RHBP has the advantage of being an extremely reliable means of achieving hardened components. However, due to the small demand for radiation hardened components and the exponentially increasing costs of advancing with Moore's law, the number of these dedicated foundries has decreased dramatically and they remain more than three generations behind state-of-the-art CMOS. RHBP is susceptible to low volume concerns such as yield, process instability and high manufacturing cost.

RHBP chipsets lag behind in time to market in comparison with in generic commercial chipsets as it involves more development time, extensive testing and budgetary requirements.

Many radhard foundries have left and continue to leave, due to reduced demand by former military and commercial customers. Presently there is only one established supplier left in Europe that is TEMIC-MHS, which has been acquired by ATMEL in 1998, a US company [10].

Radiation Hardening by Design: There has been a great deal of work on radiation hardened circuit design approaches. Rajesh[11] proposed a radiation hard PLL designed using 65nm CMOS process using circuit level hardening approach. It utilizes two independent charge pump/ low pass filter blocks, which drive two separate VCOs. The VCOs are implemented as current starved ring oscillators. But this is not radiation resistant and as the frequency increases its performance degrades due to phase noise and jitter. Boulghassoul [12] have analysed SETs effect on charge pump module. Loveless [13] presented a model to determine VCO SETs vulnerability. A VCO circuit has been designed for RHBD at circuit level for SET mitigation. Tao Wang [14] designed a radiation fault tolerant PLL design using TMR redundancy topology. Radiation hardening was obtained at architecture level. But if radiation strikes the voter circuit, PLL may fail to lock. Ozgur Cobanoglu [15] has used TMR scheme to improve SET immunity. Zhao [16] has obtained radiation hardening at circuit level by designing a novel SET resistant Complementary Current Limiter (CCL) and implemented it between charge pump and the loop filter. The CCL circuit reduces the voltage fluctuation on the input of the VCO and accelerates the PLL recovery procedure from loss of lock due to phase or frequency shift, as well as a single event strike. All of these SETs

analysis and related RHBD techniques focus on one of the sub blocks in Charge Pump PLL at a particular radiation hardening level.

RHBD techniques are incorporated in device layout or circuit architecture modifications using commercial foundries. The advantages of RHBD approach are low cost, maturity of the CMOS process and very high reputability from many silicon foundries and portability. Hence with this motivation, this work proposes to design a Radiation Hard (Radhard) Charge Pump PLL. This research work on Radhard PLL using RHBD approach can be fabricated using any existing commercial foundry, thereby reducing the manufacturing cost and time to market by avoiding the dependency on process technology and foundry.

5. Specifications of Radhard Charge Pump PLL

Referring to IEEE 2.4 GHz wireless standards Table 1 summarizes the specification of ZigBee, Bluetooth and IEEE 802.11b/g. The radhard frequency synthesizer specifications are derived from the key parameters listed in this table.

Table 1 Wireless Standards

Parameters	ZigBee	Bluetooth	802.11b	802.11g
Frequency Band (GHz)	2.4	2.4	2.4	2.4
Channel Bandwidth (MHz)	5	1	25	25
SNR (dB)	5	5	5-6	4-6
Sensitivity (dbM)	-85	-70	-76	-74
Output Power (dbM)	3	20	30	30
Settling time (us)	192	259	224	224

Considering channel bandwidth of 5MHz and SNR of 5dB, using Leeson Phase Domain model [19], the phase noise specifications can be taken as -110dBc/Hz at an offset of 10MHz. Taking Table 1 as reference, the following specifications are derived for the design of RHBD 2.4GHz Charge Pump PLL.

Table 2 Specifications of RadHard PLL

Sl No.	Parameters	Value
1	Reference Frequency	20MHz
2	Synthesized Output Frequency	2.4GHz
3	VCO Sensitivity (Kvco)	300MHz/V
4	PFD Gain (Kpd)	100uA/(2pi)
5	PLL Bandwidth (Wn)	2*pi*2MHz
6	Phase margin	60deg
7	Attenuation	20db
8	Settling Time	10us
9	Jitter	250-350ps
10	SNR	5db
11	Phase Noise	-110dbc/Hz±5dbc/Hz

Revision of previously reported works by other researches in the field of designing radhard charge pump PLL is presented in Table 3.

Table 3 Previously Reported Works Used as Reference

Frequency	Technology	Jitter	Reference
1.06 GHz	CMOS	350.35ps	[20]
200 MHz	CMOS	1.07 ns	[21]
800MHz	CMOS	-	[22]
1GHz	CMOS	227ns	[23]
1000MHz	CMOS		[24]

The number of published works in designing Radhard PLL is much more than what has been listed. We have refined the survey only for Radiation Hard by Design approach targeting only CMOS technologies.

6. Proposed Design of RHBD Charge Pump PLL

The earlier works related to RHBD techniques focused on one of the sub blocks in Charge Pump PLL at a particular radiation hardening level. Hence author proposes a design of RHBD PLL which offers radiation tolerance at all the sub blocks and across all radiation hardening levels.

A. RHBD Charge Pump PLL

Charge Pump PLL can be realized using:

1. Integer N Architecture
2. Fractional Architecture

Present work considers Integer N Architecture.

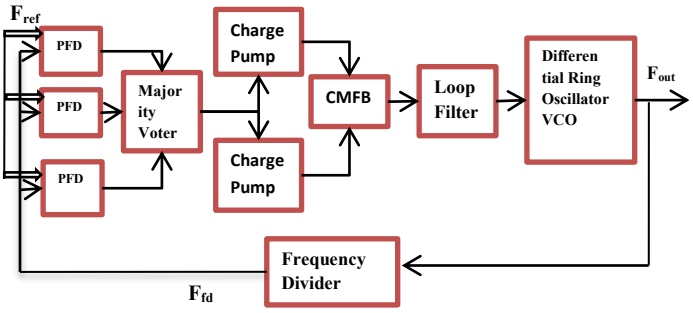

Fig 2. Functional Block Diagram of Integer N RHBD Charge Pump PLL based Frequency Synthesizer.

Design incorporates redundancy in PFD and in charge pump to increase the tolerance to radiation strikes.

The RHBD Charge Pump PLL designed has incorporated Triple Modular Redundancy (TMR) technique for the PFD block. Even if one of the PFD block is affected by the SET strike. The majority voter circuit takes the right value and sends it to the differential charge pump.

SET strike on charge pump will infuse charge which causes a mismatch in the charging and discharging currents in the charge pump circuit. The Common Mode Feedback (CMFB) circuit is used to reduce this current mismatch.

A third order loop filter is implemented as it reduces the jitter and improves the PLL performance.

Again to reduce the SET effect a fully differential ring oscillator VCO is implemented.

As it is required to compare the phase of the VCO synthesized frequency F_{out} (2.4 GHz) with the reference frequency F_{ref} (20MHz), we divide F_{out} by a factor of 120 using the frequency divider circuit.

The VCO has a centre frequency of 2.4 GHz, and range is 2.2 GHz to 2.5GHz with sensitivity of 280MHz/V

Implementations of each of these blocks are described in detail in the following sections.

B. RHBD Phase Frequency Detector Using Triple Modular Redundancy

The SET tolerant PFD circuit is designed employing the TMR technique, in which the PFD circuit, is tripled and provided to a majority voter circuit which yields the right output even in presence of SET strike as shown in the Figure 3. The circuit was tested by providing small current pulse of 1mA; 1ns pulse width at one of the PFD inputs and the circuit designed was fault tolerant and was able to give the correct output even in presence of SET. The majority voter circuit was designed using radhard logic gates.

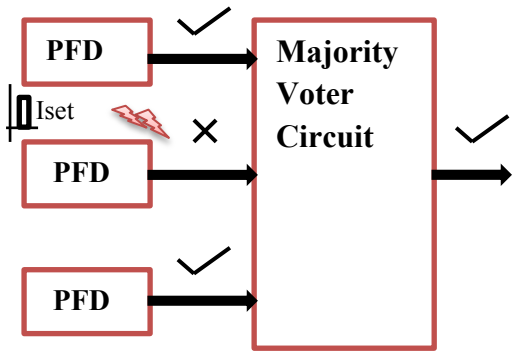

Fig 3 PFD Using TMR

The schematic diagram of the PFD circuit implemented is as shown in Figure 4.

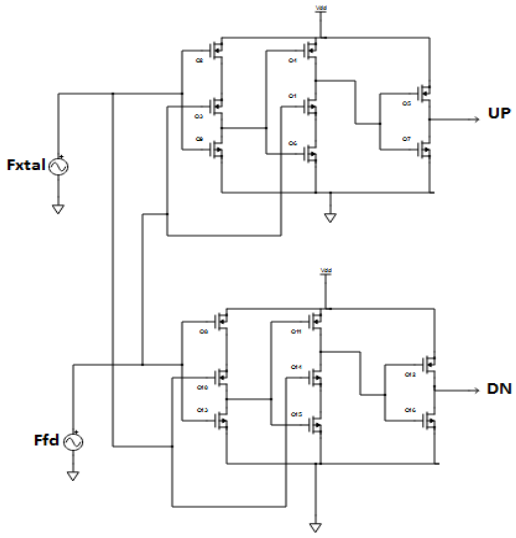

Fig 4. Schematic Diagram of the PFD

The dynamic PFD implemented eliminates dead zone. It operates at 1.8V and uses 16 transistors. The aspect ratio of all the transistors was fixed as 1.2um/180nm as it resulted in equal rise time and fall time delay.

The schematic of the majority voter circuit is given in Figure 5.

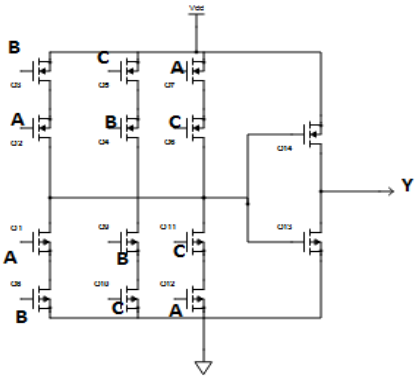

Fig 5. RHBD Majority Voter Circuit

The truth table of the Majority Voter Circuit is given in Table 4.

Table 4. Truth Table of Majority Voter Circuit

A	B	C	Y (Output)
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

The total power consumption of the entire TMR PFD circuit was measured as 76.8uW.

The simulated results of the entire RHBD PFD is as shown in Figure 6, 7 and 8.

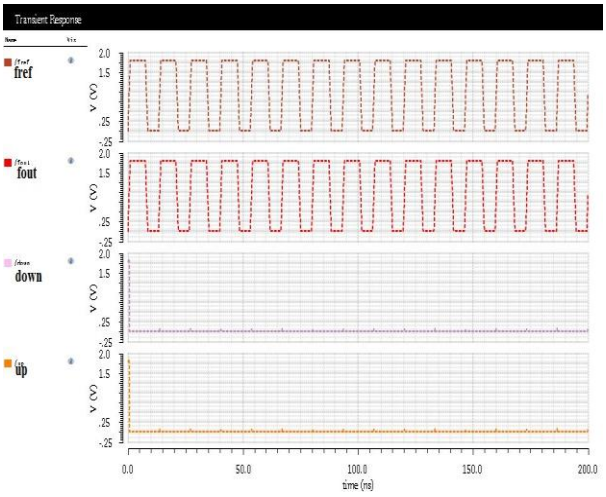

Fig 6 Output of PFD when inputs are in phase.

When both the reference input and the feedback signal from PFD are in phase, both the outputs of PFD are zero.

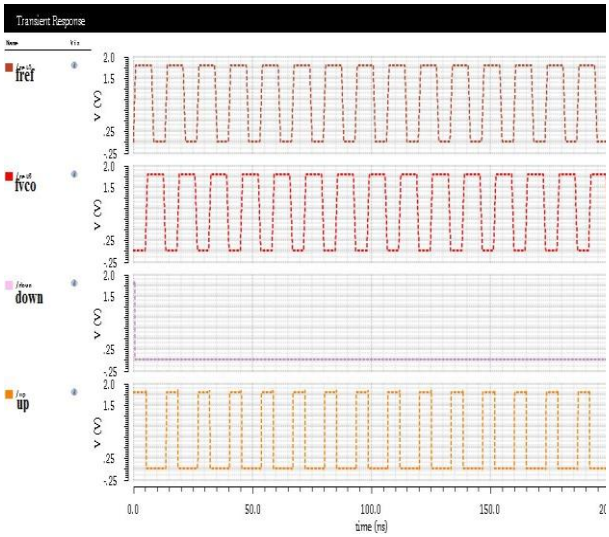

Fig 7 Output of PFD when reference input signal is leading.

When the reference input is leading, the UP signal goes high, its pulse width is proportional to the phase difference between both the signals

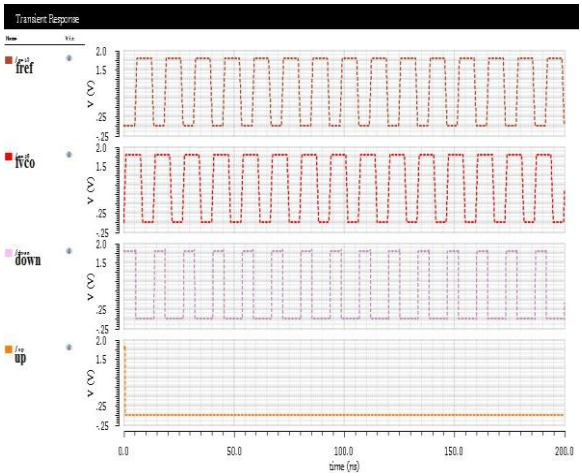

Fig 8 Output of PFD when reference input is lagging.

When the feedback signal leads, the DN signal goes high.

C. RHBD Differential Charge Pump Using Common Mode Feedback Circuit

Conventional Charge Pump circuit [26] suffers from current mismatch when hit by an SET pulse. This leads to phase noise and jitter at output signal. The present work considers using two single ended charge pump circuits. The output from the two charge pump circuits is combined through a CMFB Circuit as shown in Figure 9.

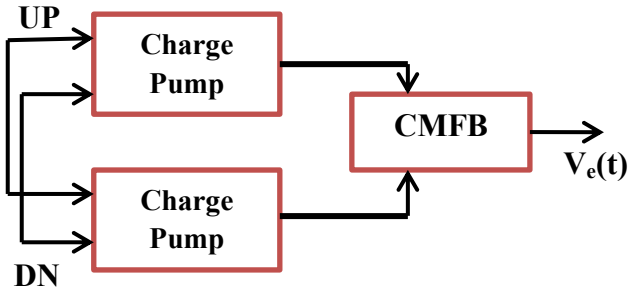

Fig 9. Differential Charge Pump Circuit with CMFB

The schematic of the single ended charge pump circuit is as shown in Figure 10.

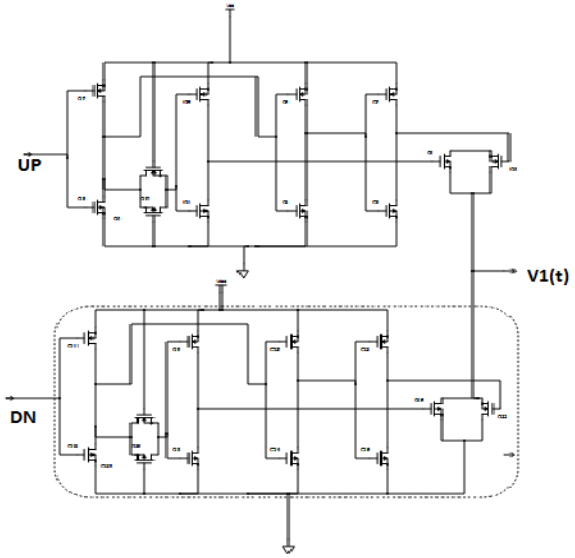

Fig 10. Single Ended Charge Pump Circuit

The SET effect can be mitigated by replacing the current source in conventional charge pump circuit by current mirror. Further mitigation is achieved by using two charge pump circuits in Dual Modular Redundancy. The outputs of the two charge pump circuits are combined using CMFB technique. The output of the charge pump $V_1(t)$ will charge when UP signal is present and discharge in presence of DN signal. The output is as shown in Figure 11 and 12.

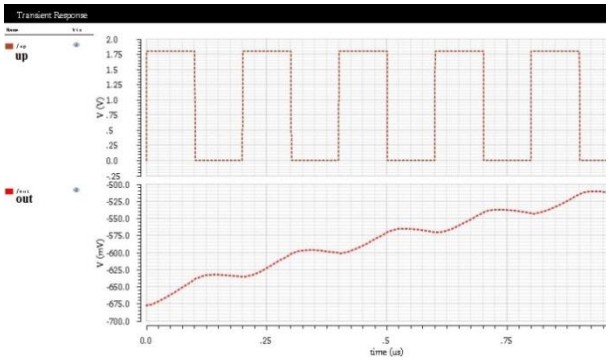

Fig 11. Charge Pump output in presence of UP signal.

In presence of SET pulse of 1mA and 1ns pulse width, there is a mismatch in charging and discharging current. The current measured in the UP branch is 171.43µA and in DN batch it is 204µA.

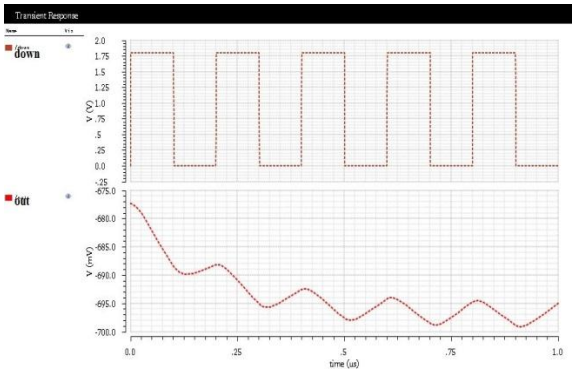

Fig 12. Charge Pump output in presence of DN signal.

The CMFB reduces the current mismatch. With CMFB the current in UP branch is 168.25µA and the current in DN branch is 167.7µA. The schematic of the CMFB circuit is as shown in Figure 13. The result of the charge pump circuit with CMFB is as shown in Figure 14 and 15.

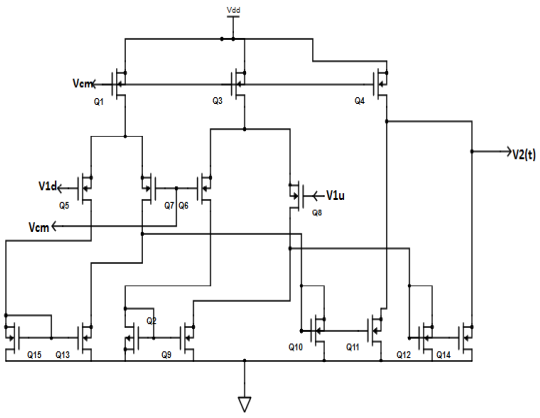

Fig 13. CMFB Circuit

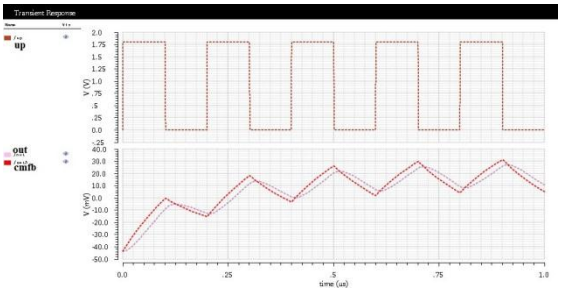

Fig 14. CMFB output during Charging cycle.

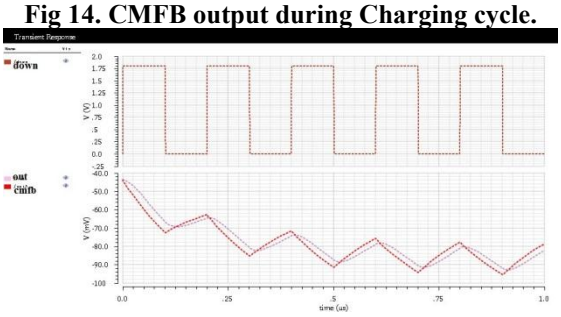

Fig 15. CMFB output during Discharging cycle.

The simulation results of PFD, Charge pump and CMFB circuit is shown in Figure 16.

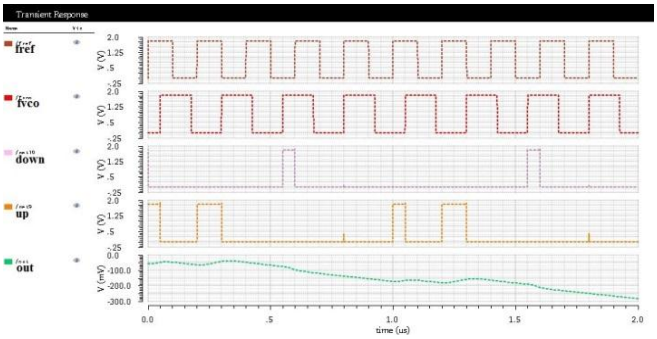

Fig 16. Simulation Result of PFD with Charge Pump.

It can be observed in Figure 16, when the UP signal is high, the charge pump circuit will be charging phase and on occurrence of DN signal pulse the discharging phase begins and this process continues iteratively. The aspect ratio of all transistors is chosen as 1.2um/0.4um. The total power consumption of the differential charge pump with CMFB circuit is 87.9uW.

D. Third Order Low Pass Passive Loop Filter Circuit

The third order loop filter components are derived using the following equations [27].

$$T1 = \frac{Sec(\emptyset p) - \tan(\emptyset p)}{wn} \quad 1$$

$$T3 = \sqrt{\frac{10^{\frac{ATTEN}{10}} - 1}{(2\pi Fxtal)^2}} \quad (2)$$

$$wc = \frac{tan\emptyset p*(T1+T3)}{(T1+T3)^2+(T1*T3)}\sqrt{1+\frac{(T1+T3)^2+(T1*T3)}{tan\emptyset p*(T1+T3)^2}} - 1 \quad (3)$$

$$T2 = \frac{1}{wc^2 * (T1+T3)} \quad (4)$$

$$C1 = \frac{T1}{T2} * \frac{Kpd*Kvco}{wc^2*N} * \sqrt{\frac{1+(wc*T2)^2}{(1+(wc*T1)^2)(1+(wc*T3)^2)}} \quad (5)$$

$$C2 = C1\left(\frac{T2}{T1} - 1\right) \quad (6)$$

$$R1 = \frac{T2}{C2} \quad (7)$$

$$C3 = \frac{C1}{10} \quad (8)$$

$$R2 = \frac{T3}{C3} \quad (9)$$

As per the specifications provided in Table 2, the loop filter components are derived as given in Table 5.

Table 5. Loop Filter Components

Sl No	Component	Value
1	R1	8.37KΩ
2	R2	0.221MΩ
3	C1	3.5pF
4	C2	102pF
5	C3	0.35pF

E. RHBD Voltage Controlled Oscillator

Radiation effect on VCO can change its centre frequency. VCO is the most sensitive part of the entire PLL circuit. The VCO must be designed in such a manner that for a given control voltage its frequency should remain unaltered in presence of SET strike. Two differential ring oscillators is implemented as VCO. The schematic of the differential ring VCO is as shown in Figure 17. The ring oscillator includes three inverter stages. Inverter implemented in each stage is rad hard.

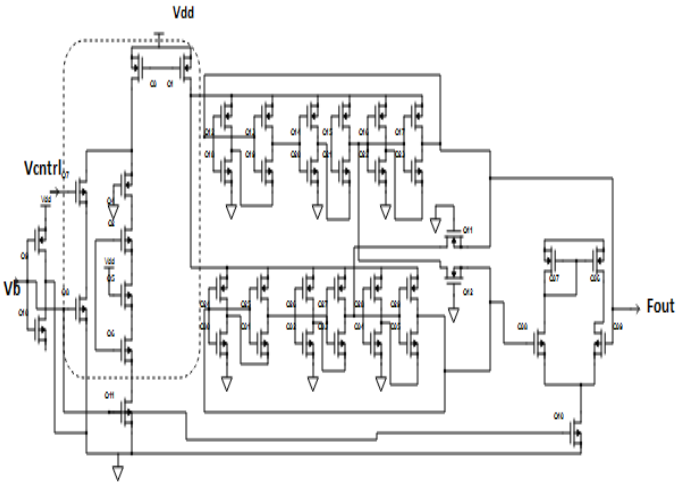

Figure 17. RHBD Differential VCO

The simulation result of the VCO is as shown in Figure 19.

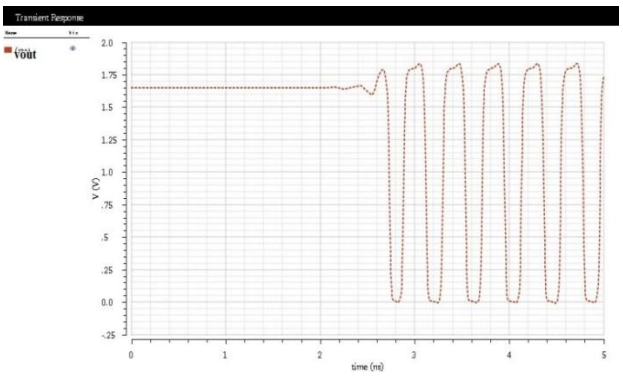

Figure 18. RHBD VCO generating 2.4GHz frequency output.

The frequency output generated by the RHBD VCO for different control voltages is provided in Table 6.

Table 6. Control Voltage Vs VCO Output Frequency

Sl No	Control Voltage (V)	Output Frequency (GHz)
1	-1.8	1.80
2	-1.6	1.98
3	-1.4	2.1
4	-1.2	2.12
5	-1.0	2.14
6	-0.08	2.376
7	-0.06	2.386
8	-0.04	2.388
9	-0.02	2.394
10	-0.01	2.397
11	-0.008	2.398
12	-0.006	2.398
13	-0.004	2.4
14	-0.002	2.4
15	-0.001	2.4
16	0.001	2.4
17	0.002	2.401
18	0.004	2.401
19	0.006	2.402
20	0.008	2.402
21	0.01	2.404
22	0.02	2.406
23	0.04	2.408
24	0.06	2.410
25	0.08	2.412
26	0.1	2.413
27	0.2	2.42
28	0.4	2.424
29	0.6	2.43
30	0.8	2.464
31	1.0	2.520
32	1.2	2.586
33	1.4	2.645
34	1.6	2.645
35	1.8	2.7

The sensitivity of the VCO from the graph of control voltage vs VCO frequency shown in Figure 19 is calculated to be 280MHz/V.

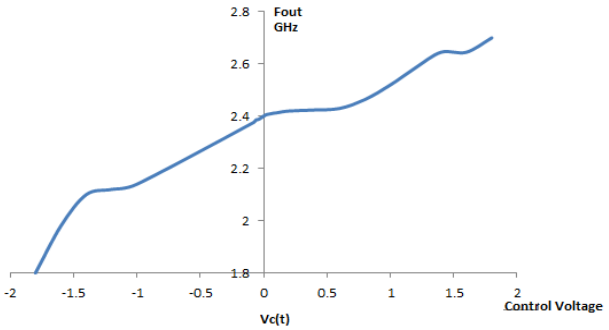

Fig 19. VCO Characteristics

F. RHBD Frequency Divider

The VCO frequency is divided by the Frequency Divider circuit by a factor of 120. The divided output frequency F_{fd} is fed to the PFD, where it is compared with the input frequency F_{xtal} to compute the phase difference. The Frequency Divider (FD) circuit is built using D Flip Flop. Each FD circuit divides the output frequency by a factor of 2. Hence we need 7 stages of FD circuit to divide 2.4GHz VCO frequency to make a comparison with 20 MHz $F_{xtal.}$ The schematic of the FD circuit is shown in Figure 20.

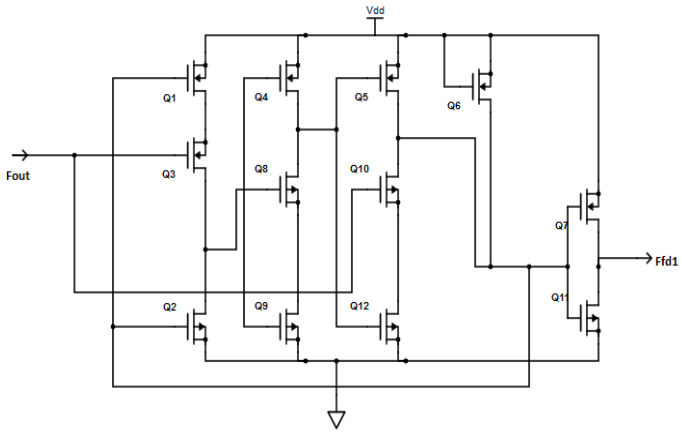

Fig 20. RHBD Frequency Divider Circuit

The complete simulation results of all seven stages of the FD circuit are as shown in Figure 21.

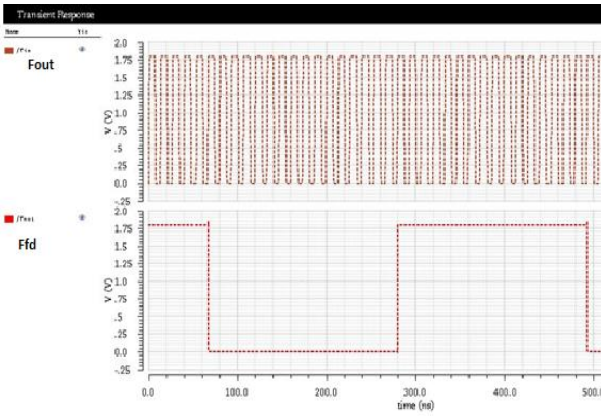

Fig 21. Simulation Result of the Frequency Divider

7. Results and Discussion

The simulation result of the complete RHBD Charge Pump PLL is shown in Figure 22.

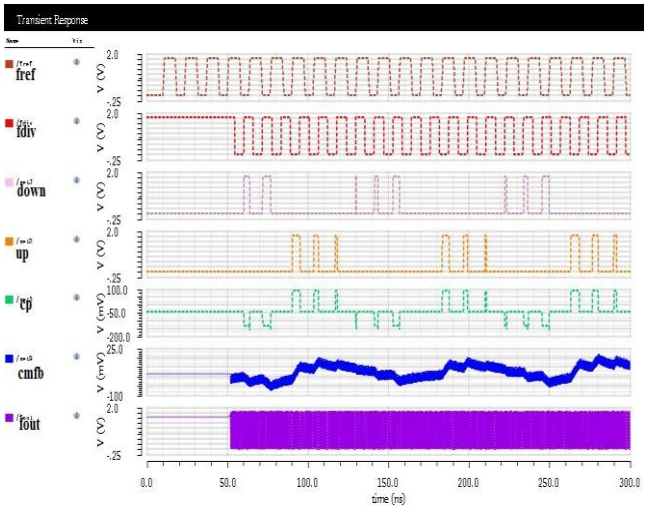

Fig 22. Simulation result of the complete RHBD Charge Pump PLL circuit.

The results obtained against the specification are as provided in Table 7.

Table 7. Results of the RHBD Charge Pump PLL

Sl No	Parameter	Specification	Simulation Results
1	Input Frequency	20MHz+/-5MHz	20MHz input
2	Output Synthesized Frequency	2.2GHz-2.5GHz	2.4GHz
3	VCO Sensitivity	300MHz/V	280MHz/V
4	Loop Filter Type and Order	3rd Order	3rd Order RC filter
5	Settling Time	<10us	52ns
6	Rms jitter	<200ps	8ps
7	SET Impulse Noise	1ns, 1mA input	1ns, 1mA input
8	Settling time with noise	<100us	159ns
9	Rms jitter in presence of SET impulse noise	250-350ps	128.9ps
10	Phase Noise	110dbc/Hz±5dbc/Hz	-118.1dbc/Hz
11	Phase Noise in presence of impulse noise	110dbc/Hz±5dbc/Hz	-94.03dbc/Hz
12	Power	1W	1.39mW

The jitter characteristics when the PLL is struck by SET pulse at the PFD, charge pump, loop filter and VCO nodes are summarized in Table 8.

Table 8. Jitter Statistics of PLL when struck by SET pulse.

Sl No.	SET Strike No.	Node	Tmax (ps)	Tmin (ps)	Period Jitter (ps)
1	1	Charge Pump1UP input	425	370	55
2		Charge Pump1DN input	425	404	41
3		Charge Pump 1 output	417	360	57
4		Charge Pump2UP input	417	359	58
5		Charge Pump2DN input	420	361	59
6		Charge Pump 2 output	418	377	41
7		CMFB output	418	366	52
8	2	Charge Pump1UP input	420	366	54
9		Charge Pump1DN input	420	371	49
10		Charge Pump 1 output	417	359	58
11		Charge Pump2UP input	418	359	59
12		Charge Pump2DN input	418	367	51
13		Charge Pump 2 output	420	369	51
14		CMFB output	420	367	53
15	3	Charge Pump1UP input	420	375	45
16		Charge Pump1DN input	417	368	49
17		Charge Pump 1 output	418	359	59
18		Charge Pump2UP input	417	358	59
19		Charge Pump2DN input	419	368	51
20		Charge Pump 2 output	420	369	51
21		CMFB output	420	368	52
22	1	PFD1 input	417	362	55
23		PFD1 output	417	369	48
24		PFD2 input	417	362	55
25		PFD2 output	417	369	48
26		PFD3 input	418	363	55
27		PFD3 output	418	370	48
28		Majority Voter circuit output	417	366	51
29	2	PFD1 input	417	361	56
30		PFD1 output	417	368	49
31		PFD2 input	417	362	55
32		PFD2 output	417	369	48
33		PFD3 input	418	372	46
34		PFD3 output	417	368	49
35		Majority Voter circuit output	417	365	52
36	3	PFD1 input	417	361	56
37		PFD1 output	417	368	49
38		PFD2 input	417	361	56
39		PFD2 output	417	368	49
40		PFD3 input	417	361	56
41		PFD3 output	417	368	49
42		Majority Voter circuit	420	367	53

		output			
43	1	Loop Filter input	420	368	52
44		Loop Filter Output	425	370	55
45	2	Loop Filter input	420	368	52
46		Loop Filter Output	422	366	56
47	3	Loop Filter input	421	369	52
48		Loop Filter Output	425	369	56
49	1	VCO input	425	369	56
50		VCO differential ring 1 stage 1 inverter input	421	373	48
51		VCO differential ring 1 stage 2 inverter input	425	373	52
52		VCO differential ring 1 stage 3 inverter input	427	375	52
53		VCO differential ring 1 stage 1 inverter output	421	369	52
54		VCO differential ring 1 stage 2 inverter output	421	369	52
55		VCO differential ring 1 stage 3 inverter output	421	368	53
56		VCO differential ring 2 stage 1 inverter input	423	375	48
57		VCO differential ring 2 stage 2 inverter input	424	372	52
58		VCO differential ring 2 stage 3 inverter input	425	373	52
59		VCO differential ring 2 stage 1 inverter output	421	369	52
60		VCO differential ring 2 stage 2 inverter output	423	371	52
61		VCO differential ring 2 stage 3 inverter output	422	369	53
62		VCO output	425	371	54
63	2	VCO input	427	371	56
64		VCO differential ring 1 stage 1 inverter input	427	370	57
65		VCO differential ring 1 stage 2 inverter input	427	379	48
66		VCO differential ring 1 stage 3 inverter input	425	373	52
67		VCO differential ring 1 stage 1 inverter output	421	369	52
68		VCO differential ring 1 stage 2 inverter output	421	369	52

69		VCO differential ring 1 stage 3 inverter output	425	372	53
70		VCO differential ring 2 stage 1 inverter input	425	397	48
71		VCO differential ring 2 stage 2 inverter input	427	375	52
72		VCO differential ring 2 stage 3 inverter input	425	372	53
73		VCO differential ring 2 stage 1 inverter output	425	373	52
74		VCO differential ring 2 stage 2 inverter output	425	372	53
75		VCO differential ring 2 stage 3 inverter output	425	371	54
76		VCO output	427	372	55
77	3	VCO input	425	369	56
78		VCO differential ring 1 stage 1 inverter input	425	368	57
79		VCO differential ring 1 stage 2 inverter input	425	367	58
80		VCO differential ring 1 stage 3 inverter input	427	375	52
81		VCO differential ring 1 stage 1 inverter output	425	373	52
82		VCO differential ring 1 stage 2 inverter output	425	373	52
83		VCO differential ring 1 stage 3 inverter output	421	368	53
84		VCO differential ring 2 stage 1 inverter input	421	369	52
85		VCO differential ring 2 stage 2 inverter input	425	372	53
86		VCO differential ring 2 stage 3 inverter input	424	372	52
87		VCO differential ring 2 stage 1 inverter output	424	371	53
88		VCO differential ring 2 stage 2 inverter output	423	370	53
89		VCO differential ring 2 stage 3 inverter output	425	370	55
90		VCO output	427	372	55

8. Conclusion

The PLL circuit is sensitive to radiation effect. SET strike on the PLL can cause the PLL to malfunction. In this paper a novel RHBD Charge Pump PLL is designed. The Charge pump model implemented in Cadence in absence of SET noise had rms jitter of 8ps, phase noise of -118.1dbc/Hz and settling time of 52ns, in presence of noise, the rms jitter was recorded as 128.9ps, phase noise of -94.03dbc/Hz and settling time is 159ns. SET pulse is injected in 90 different nodes randomly to measure period jitter. The minimum measured period jitter was 41ps and maximum measured jitter was 59ps.

Using CMFB, the current in charge pump UP and DN branches were measured to be 168.25µA and 167.7µA, without CMFB the charge pump UP and DN current were 171.43µA and 204µA thereby indicating CMFB reduces current mismatch.

The VCO has a tuning range 1.8GHz to 2.7GHz with a centre frequency of 2.4GHz. The VCO sensitivity obtained is 280MHz/V.

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