Quasi Resonant Flyback Topology Based LCD TV Power Supply Board Design and Power Loss Analysis

YUNUS SAHIN[1], GULAY TOHUMOGLU[2]
[1]Department of Electrical-Electronic Engineering
Dokuz Eylül University, Izmir, TURKEY

[2]Department of Electrical-Electronic Engineering
Dokuz Eylül University, Izmir, TURKEY

Abstract: - Usage of the consumer electronics products such as TVs has increased rapidly with the emerging technological developments recently, hence limiting the power consumption of such devices have become more and more crucial. Switched Mode Power Supply (SMPS) topologies that allow higher efficiency than linear supplier became prevalent after the 1960s. Flyback converter is one of the SMPS topologies and very popular in low power applications because of multiple outputs, design simplicity and low cost. In this work, quasi resonant switching based flyback converter is analyzed, design equations extracted and designed with given parameters. Also power loss model of converter is analyzed and verified with practically results.

Key-Words: - SMPS, Quasi Resonant Flyback, power loss model

1 Introduction

Thanks to the advances in semiconductor technology, instead of linear power devices, switched mode power supplies allowing the design of smaller electronic boards which are more efficient have been widely used [1].

There are different types of switched mode power supply topologies. Flyback converter is the most preferred topology for low power applications that require power less than 150W with its ease of design, cost-effectiveness and capability of providing multiple isolated outputs [2]. Thanks to these properties flyback converters are mostly preferred in power board design for LCD TVs. Since the demand for small size, low weight and low cost solutions in LCD TVs is increasing, the tendency to use switching mode power supplies at higher frequencies [3]. However, as switching frequency increases, switching losses and effects of parasitic components increase. Because of these drawbacks efficiency and power capacity decrease.

Operation of the flyback converter is based on the energy storage principle of the coupled inductor (also referred to as flyback transformer). In Fig. 1, power circuit of the flyback converter is shown.

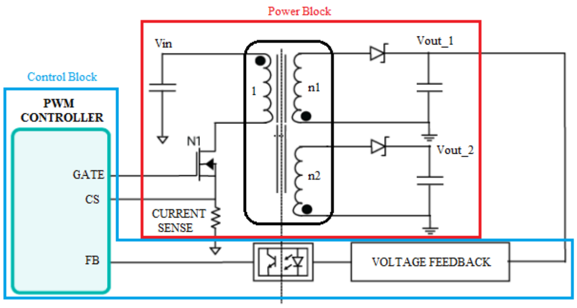

Fig. 1. Flyback circuit with two outputs

Switching loss and MOSFET voltage stress are very important parameters in designing the flyback converter. These parameters are increasing due to the leakage inductance of the coupled inductor of flyback [4]. Soft switching methods are proposed to minimize the switching losses due to high frequency [5].

Quasi-resonant switching utilizing the existing L and C components in the circuit, is one of the proposed soft switching methods. When the secondary winding current reaches to zero, magnetized inductance (L) of the coupled inductor and total output capacitance (C) of the MOSFET cause oscillations in drain-source voltage of the

MOSFET. Quasi-resonant switching method uses this oscillation to allow MOSFET to switch ON while the drain-source voltage is minimum. Thanks to this method, the switching losses are minimized [6]. In Fig. 2, drain-source voltage and gate signal of MOSFET is shown for the discontinuous conduction mode.

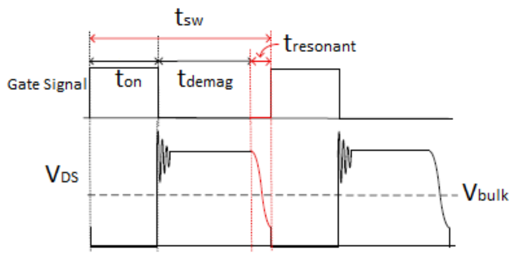

Fig. 2. Gate signal and Vds voltage for discontinuous conduction mode

In the continuous conduction mode, since the MOSFET switches OFF before secondary winding current reaches to zero, there is no time interval for oscillations in MOSFET's drain-source voltage to occur. Therefore, quasi-resonant switching is a method can be used only in discontinuous conduction mode and boundary conduction mode. Current-voltage waveforms for CCM and DCM are given in Fig.3.

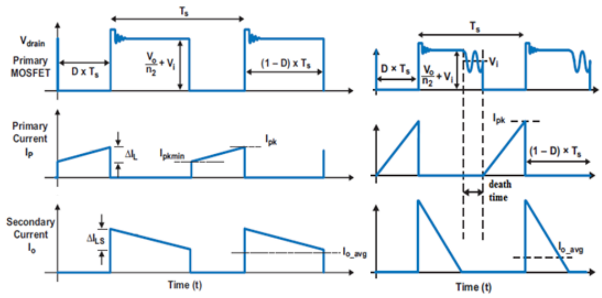

Fig. 3. Current-voltage waveforms for continuous (left) and discontinuous (right) conduction modes

Besides having advantages such as ease of design, cost-effectiveness and capability of providing multiple isolated outputs similar to traditional flyback converter, quasi-resonant flyback has lower switching loss compared to the traditional flyback since soft-switching method is utilized. The comparison of different flyback topologies is given in Table 1 [7].

Table 1. Comparison of Flyback Converter Topologies

Parameter	***FF DCM***	***FF CCM***	***QR***
MOSFET Switch On Loss	Low	Highest	Lowest
Conduction Loss	Highest	Low	High
Output Diode Reverse Recovery Loss	Virtually Zero	High	Virtually Zero
Efficiency	Low	High	Best

In the scope of this study, quasi resonant converter is chosen considering its high efficiency compared to other topologies. This research work aims at design and implementation of two outputs quasi resonant based flyback converter in discontinuous conduction mode and also perform power loss analysis of designed power board. There are two secondary outputs in the design, where one output is 12V and the other is 24V. Voltage regulation is achieved by the feedback from 12V output. This output is used for supplying the digital units of the TV. The 24V output is utilized for backlighting unit of the TV.

2 Methodology

2.1. Quasi Resonant Flyback Design

In this study, a MOSFET with 750V maximum drain-source breakdown voltage is used as switch. Maximum breakdown voltage criteria of the MOSFET is taken as a reference for calculating transformer turn ratio of the coupled inductor.

1) Determining the Turn Ratio: For reliability reasons, maximum voltage stress on MOSFET operating at steady state is taken as less than 80% of the rated MOSFET voltage. Therefore, the equation given below (1) should be satisfied:

$$V_{DCmax} + 2.5\, x\, n\left(V_o + V_{d,fw}\right) \leq 0.8\, x\, V_{DSmax} \qquad (1)$$

In this equation, V_{DCmax} is the maximum value of the input voltage, V_o is output voltage, $V_{d,fw}$ is the voltage drop on output diode when conducting, n is the ratio of primary winding to secondary winding and V_{DSmax} is maximum breakdown voltage of the MOSFET.

2) Calculation of D_{max}: The maximum duty cycle (D_{max}) of is calculated via (2) thanks to the transfer function of the flyback converter [8]:

$$D_{max} = \frac{1}{1 + \frac{V_{in}}{n * V_{out}}} \tag{2}$$

3) Calculation of Primary Inductance: While MOSFET is conducting, primary winding current increases linearly. Primary current reaches its peak value when the MOSFET switches OFF. Primary current peak value is calculated with (3) as follows:

$$I_{pri,pk} = \frac{T_s * V_{DC,min} * D}{L_p} \tag{3}$$

L_p is the primary inductance of the coupled inductor, T_s is switching period, $V_{DC,min}$ is the minimum value of the input voltage.

When MOSFET switches OFF, the energy stored in the air gap and the core is transferred to the secondary winding [9]. During this period, the load and the output capacitor are supplied through the output diode. Peak value of the secondary current is calculated with (4):

$$I_{sec,pk} = \frac{T_s * V_{out} * D2}{L_s} \tag{4}$$

L_s is the secondary inductance of the coupled inductor, V_{out} is the output voltage, $D2$ is the ratio of MOSFET's OFF duration to the switching period.

Rearranging the (3) and (4) to isolate D and D2 leads to (5) and (6).

$$D = L_p \frac{I_{pri,pk}}{T_s * V_{DC,min}} \tag{5}$$

$$D2 = L_s \frac{I_{sec,pk}}{T_s * V_{out}} \tag{6}$$

In discontinuous conduction mode, sum of the MOSFET's ON and OFF durations should be less than the switching period. Therefore, for the discontinuous conduction mode, the following (7) should be satisfied.

$$D + D2 \leq 1 \tag{7}$$

The transfer function for discontinuous operation mode is given as follows (8):

$$\frac{V_{out}}{V_{DC,min}} = \frac{D}{n * D2} \tag{8}$$

Value of the primary inductance for discontinuous operation is calculated with (5), (6), (7) and (8).

$$L_p \leq \frac{(V_{DC,min} * D)^2}{2 * P_{out} * f_s * (D + D2)} \tag{9}$$

Since D2 is equal to $1 - D_{max}$ for the critical conduction mode, primary inductance value is calculated by changing D with D_{max} with (10).

$$L_p = \frac{(V_{DC,min} * D_{max})^2}{2 * P_{out} * f_s} \tag{10}$$

4) Calculation of minimum number of primary turns: The maximum flux density swing in normal operation should be considered while designing the transformer. From Faraday's law, the minimum number of turns for the transformer primary side is calculated by (11):

$$N_{p,min} = \frac{L_m * I_{pri,pk}}{B_{max} * A_e} 10^6 \tag{11}$$

In (11), A_e is cross sectional area of the core, B_{max} is maximum flux density, $N_{p,min}$ is minimum number of primary turns. B_{max} is generally chosen as 0.3 – 0.4T.

5) Calculation of the number of turns for outputs: Once the number of primary turns and transformer turn ratio is calculated, the number of secondary turns is calculated with (12).

$$n = \frac{Np}{Ns} \tag{12}$$

In designs with different output voltages, number of secondary turns of different outputs is calculated with (14).

$$N_{s,n} = \frac{V_{out,n} + V_{d,n}}{V_{out,1} + V_{d,1}} N_{s,1} \quad (13)$$

In (13), $N_{s,n}$ is the number of secondary turns, $V_{out,n}$ is output voltage, $V_{d,n}$ is the voltage drop across the rectifier diode used for output voltage while conducting.

6) Selection of the output diode: The rectifier diode to be used at the secondary side should be able to withstand voltage and current stress. The voltage across the output diode when it is in off state is calculated with (14):

$$V_{rev,diode} = V_{out} + V_{DC,max} * \frac{N_s}{N_p} \quad (14)$$

In (14), $V_{rev,diode}$ is the voltage stress that the diode is exposed to when it is in off state.

The selected diode should have enough margins in order not to cause any breakdown. Nominal voltage of the selected diode should be higher than the sum of the safety margin and the voltage stress calculated with (14). The safety margin is taken as 30% in this study. Hence, the nominal voltage of the selected diode is calculated with (15):

$$V_{rated,diode} = 1.3 * V_{rev,diode} \quad (15)$$

7) Selection of the output capacitor: Output capacitor supplies the required energy for the load while the output diode is not conducting. Charge-discharge graph of the output capacitor is given in Fig. 4.

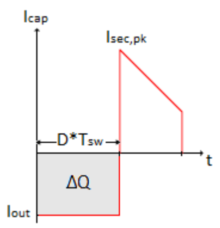

Fig. 4. Charge-discharge graph of the output capacitor

Charge-voltage equation of the capacitor is given below (16):

$$\Delta Q = \Delta V_{out} * C_{out} = D * T_{sw} * I_{out} \quad (16)$$

In (16), ΔV_o is the ripple voltage of the capacitor, C_o is the value of the output capacitance. Value of the minimum output capacitance can be calculated by (17), by rearranging the (16):

$$C_{min} = \frac{D * I_{out}}{\Delta V_{out} * f_{sw}} \quad (17)$$

In (17), f_{sw} is the switching frequency. Another important factor for choosing the capacitor is the ripple current value. The value of the ripple current depends on the operation frequency and temperature. The ripple current value of the capacitor to be chosen can be calculated by (18).

$$I_{C,RMS} = \sqrt{(I^2_{sec,RMS} - I^2_{out})} \quad (18)$$

The circuit elements chosen as discussed above are assembled in accordance with the scheme given in Fig. 1 and quasi-resonant flyback converter design is implemented by using FAN6300A PWM controller. Design specifications and parameter values are given in Table II and Table III respectively.

Table 2. Design Specifications

Design Specifications	
Parameter	***Value***
Nominal input voltage	220-240Vac
Maximum input voltage	176-264Vac
Input voltage frequency	50-60Hz
Output Voltages	12V and 24V
Output Currents	2A for 12V 1.5A for 24V

Table 3. Design Parameters

Design Parameters	
Parameter	***Value***
Primary inductance	400µH ±%10
Number of primary turns	52
Number of secondary(12V) turns	7
Number of secondary(24V) turns	14
Output capacitance (12V)	25V 1000µF 1.9A (x2 parallel)
Output capacitance (24V)	50V 680µF 2.3A
Output diode (12V)	100V 5A
Output diode (24V)	150V 5A

Design Parameters	
Parameter	***Value***
Core	KP95

2.2. Power Loss Analysis

The Fig. 5 and the Fig. 6 shows the loss equivalent circuit of flyback converter.

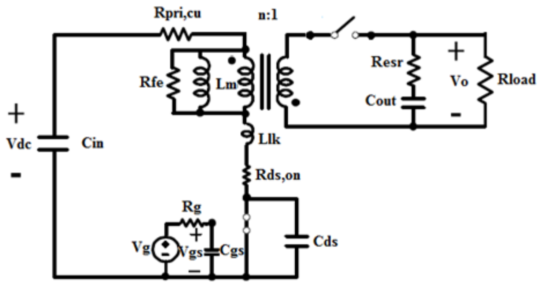

Fig. 5. Loss equivalent circuit of flyback while switch is turned on

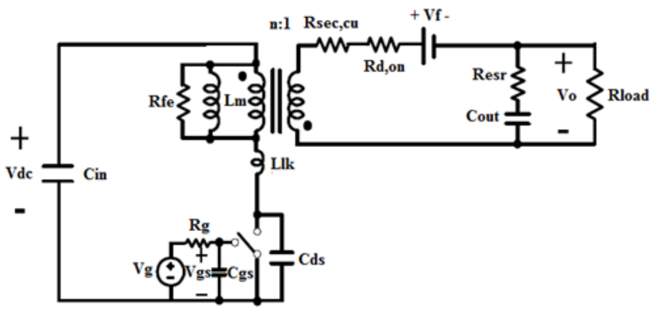

Fig. 6. Loss equivalent circuit of flyback while switch is turned off

Losses taken into account and potential loss calculations are as follows.

8) Transformer Losses: Transformer losses are examined under three subtitles as core loss, copper loss and leakage inductance loss.

Core loss is calculated by (19).

$$P_{fe} = P_{cv} * A_e * l_e \quad (19)$$

In (19), A_e is the cross sectional area of the core, l_e is the length of the core, P_{cv} is the power loss per volume depending on the frequency and maximum flux density. P_{cv} is determined thanks to the graph given in Fig. 7 which is provided by the manufacturer.

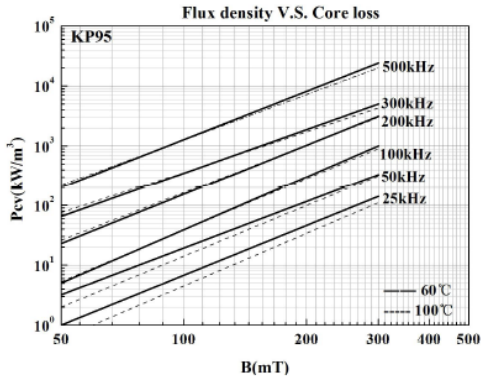

Fig. 7. Core loss vs flux density graph of the KP95 core for different frequencies

For calculating the copper loss, winding resistance is obtained by (20).

$$R_{i,DC} = \rho \frac{MLT * N_i}{A_{wire,i}} \quad (20)$$

In (20), $R_{i,DC}$ i is the winding resistance, ρ is the resistivity of the conductors and MLT is the mean turn length.

The copper loss is calculated by using the winding resistance and current value together as given in (21).

$$P_{cu} = I_i^2 * R_{i,DC} \quad (21)$$

Leakage inductance loss is calculated by (22).

$$P_{leak} = \frac{1}{2} I_{pri,pk}^2 * L_{leak} * f_{sw} \quad (22)$$

9) MOSFET losses: MOSFET losses are examined in two subtitles as R_{DSon} loss and switching loss. R_{DSon} loss is calculated by (23).

$$P_{on} = I_{pri,rms}^2 * R_{DS,on} \quad (23)$$

In (23), $I_{pri,rms}$ is the RMS value of the current through the primary winding.

Switching loss is calculated by the (24) assuming that the current-voltage transition is linear.

$$P_{tot,sw} = \frac{V_{DS} I_D (T_{off} + T_{on})}{6} f_{sw} \quad (24)$$

10) ESR loss of the output capacitor: Power loss due to equivalent series resistances of the capacitors is calculated by (25).

$$P_{cap,ESR} = I_{C,rms}{}^2 * R_{ESR} \quad (25)$$

11) Output rectifier diode loss: Power loss on the output rectifier diode which stems from the voltage drop when it is conducting is calculated by (26).

$$P_{diode,loss} = V_f * I_{D,RMS} \quad (26)$$

12) Current sense resistor loss: Power loss on the sense resistor serially connected to the MOSFET in order to monitor the primary winding current is calculated by (27).

$$P_{sense} = I_{pri,rms}{}^2 * R_{sense} \quad (27)$$

Power losses due to the reasons explained above are summarized in Fig. 8. Total power loss is calculated as 10.09W. The efficiency is calculated as 85.6 % at maximum load condition. Efficiency results obtained for different input voltages and load conditions are given in Table IV. For nominal input voltage (220 Vac) and maximum output power, efficiency is calculated as 85.9%. For input voltages of 176Vac and 264Vac and maximum load condition, the efficiencies are calculated as 84.6% and 86% respectively.

Table 4. Efficiency vs Input Voltage

	EFFICIENCY		
Pout (W)	176Vac	220Vac	264Vac
60	0.846	0.859	0.86

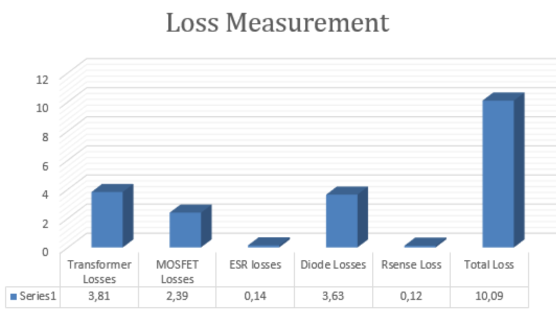

Fig. 8. Calculated power losses on the circuit elements

3 Conclusion

A detailed design procedure of flyback converter for DCM operation is presented. An example power board that has two outputs is constructed. Also power loss analysis is done for transformer, MOSFET, rectifier diode, sense resistor and output capacitors. The calculated losses are closely matching with measured losses. The results present that, proposed flyback converter is good choice for isolated DC-DC converters with low power applications.

References

[1] Chung, H., Hui, S.Y.R. and Wang, W.H., "An Isolated Fully Soft-Switched Flyback Converter with Low Voltage Stress", *IEEE PESC*, Vol. 2, 1417-1423, 1997.

[2] Ridley, R. B., Lotfi, A., Vorperian, V., and Lee, F. C., "Design and control of a full-wave quasi-resonant flyback converter", *EEE APEC Proceedings*, 41-49, 1988.

[3] Liang S.-A., "Design Optimization for LCD TV Power Supply with Resonant Technique", *IEEE PESC*, 702-707, 2007.

[4] Liu K., Oruganti R., & Lee F.C., "Resonant Switches - Topologies and Characteristics", *IEEE PESC*, 106-116, 1985.

[5] Fanington, R., Jananovi, M.M., & Lee, F.C., "A new family of isolated converters that uses the magnetizing inductance of the coupled inductors to achieve zero-voltage switching", *IEEE Truns. Power Electron*, Vol. 8, No. 4, 535-545, 1993.

[6] Chen, K. H., & Liang T. J., "Design of Quasi-Resonant Flyback Converter Control IC with DCM and CCM Operation" *International Power Electronics Conference (IPEC-Hiroshima 2014 - ECCE ASIA)*, 2750-2753, 2014.

[7] Infineon.com, "Quasi-resonant and fixed-frequency flyback comparison", 2018. [Online]. Available: https://www.infineon.com/dgdl/Infineon-Infineon-ApplicationNote_Quasi_resonant_and_fixed_frequency_flyback_comparison-AN-v01_00-EN.pdf?fileId=5546d46267354aa001673e54d82e5e90. [Accessed: 06-Dec-2018].

[8] N. Mohan, T. Udeland., and W. Robbins, "Power Electronics: Converters, Applications and Design", *3rd ed. New York, Wiley*, 2003.

[9] Yao, K., Fu, X., and Lv, J., "DCM Flyback PFC Converter with Optimum Utilization Control of Switching Cycles", *IEEE Energy Conversion Congress and Exposition*, 2445-2452, 2015.