Design and Simulation of Decimator for Digital Signal Processing

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Abstract: Decimator is a significant sampling device utilized for multi-rate applications in digital signal handling. Multirate signal processing demands high performance decimator with less resources and computation requirements for cost effectiveness. So, an efficient decimator has been designed in this paper to lessen the resources and computation requirements. The multistage decimator models have been designed and analyzed utilizing three distinct procedures. The performance of designed decimators is compared in terms of required number of multipliers, adders, multiplication per input sample (MPIS) and addition per input sample (APIS). It has been seen that the performance of all the designs are according to characterized details however number of required resources and computations varies significantly. The Nyquist design implementation lessens multiplier and adder utilization by 64.25 % and 64.68 % individually. This proposed design likewise shows decrease in MPIS and APIS by 53.85 % and 56.54 % separately when contrasted with half band design to provide high-performance cost-effective solution for multirate applications.

Key-Words: Addition Per Input Sample, Digital Signal Processing, Decimator, Finite Impulse Response Filter, Half Band Filter, Multiplication Per Input Sample, Nyquist Filter, Multi Rate Filter

Received: July 25, 2023. Revised: May 12, 2024. Accepted: June 15, 2024. Published: July 23, 2024.

1. Introduction

The boundless utilization of advanced portrayal of signals for transmission and capacity has made difficulties in the space of digital signal handling [1]. Accomplishing the fundamental performance characteristics requires cautious thought of a few significant variables, including filter architecture and digital filter design techniques [2]. The uses of digital FIR filter in up and down sampling strategies are followed everywhere in modem electronic items. For each electronic item, lower circuit intricacy is dependably a significant design focus since it decreases the expense [3]. There are numerous applications where the sampling rate should be changed. Interpolators and decimators are used to incline or decline the sampling rate [4]. Discrete time structures with inconsistent sampling rates at different parts are called Multi rate structures. Multirate structures or frameworks are building blocks regularly utilized in digital signal processing (DSP). Their capability is to modify the rate of the discrete-time signals, by inserting or removing a part of the signal samples. They are fundamental in different standard signal handling methods, for example, signal inspection, de-noising, compression, etc.

Multirate frameworks have progressively tracked down applications in new and arising areas of signal handling, as well as in a few adjoining disciplines like wireless communication. The multirate DSP in the correspondence frameworks effectively gives extra levels of opportunity in the design of the receivers. One more significant class of multirate structures is utilized at the transmitter side to introduce the redundancy in the information stream. This redundancy for the most part works with the equalization process by compelling specific construction on the sent signal. Assuming the channel is unknown, this system assists with recognizing it; in the event that the channel is ill conditioned, extra redundancy dodges serious noise amplification at the receiver.

The submerged communication structure needs a straightforward, low-power structure since it is hard to supplant a power supply and a battery because of establishment climate requirements. Thus, a low intricacy and low-power utilization digital down converter is required [5]. In numerous applications of communication and signal handling frameworks, a narrowband signal of interest is separated from a wideband signal utilizing filter circuit of receivers. In wireless communication receivers, the multirate filter circuits are used for this purpose. Accordingly, these multi-rate filter networks are planned and carried out with its identical digital counterpart [6]. Multi rate filtering technique is utilized to achieve high-resolution. It can diminish the intricacy of the circuit and furthermore the overall power consumed [7].

The frequency of occurrence of a signal can be differed, by utilizing Multi Rate Framework. A multi rate framework might have different sampling rates at various phases of process by permitting the sampling frequency to be diminished or expanded without huge bothersome impacts of errors like quantization and aliasing [8]. This rate change necessity prompts

creation of undesired signals related with aliasing and imaging errors. So some sort of filter ought to be set to lessen these errors [9]. There are two fundamental sampling rate modification gadgets in addition to conventional elements like a multiplier, and a delay. Delta sigma converters can be divided into two primary structure blocks: modulator and decimation filter. With a decent comprehension of these structure hinders a robust and effective design can be created [10].

2. Decimators

Software defined radio (SDR) is a radio wherein the properties of carrier frequency, signal data transfer capacity, modulation and a few different parameters are characterized by software. Typical FIR structures and its variations fail to work at such high frequencies [11]. The digital signal processing application by utilizing variable sampling rates can improve the flexibility of software defined radio. It decreases the requirement for costly anti-aliasing analog filters and empowers handling of various kinds of signals with various sampling rates. It permits dividing of the high-speed processing into parallel multiple lower speed processing tasks which can prompt a huge saving in computational power and cost.

Wideband receivers exploit multirate signal processing for effective channelization and offers adaptability for symbol synchronization. The ordinary interpolator and decimator are carried out by utilizing direct form FIR filter structure. The issue with implementing sampling rate convertor utilizing direct structure was that filter length straightly increments with the decimation and Interpolation rate. Hence resource usage additionally expands; this thus increments power utilization, area requirement and delay of the sampling rate convertor [12].

The precise design of a decimation filter is of prime significance since it manages the attenuation of undesirable aliasing [13]. The significant prerequisites for the design and implementation of the decimators are high speed, low power utilization and low signal distortion [14]. Ordinarily decimation filters are achieved by utilizing finite impulse response (FIR) filters because of their linear phase and stability in nature [15]. Parallel polyphase filters are normally used to execute decimation as they give low complexity and can be carried out efficiently [16]. Normally lowpass filters are utilized for decimation and interpolation. While decimating, lowpass filters are utilized to decrease the bandwidth of a signal before decreasing the sampling rate. This is done to limit aliasing because of the decrease in the sampling rate. While decimating, the bandwidth of a signal is decreased to a proper worth so negligible aliasing happens while decreasing the sampling rate.

Down sampler is essential sampling rate change device used to decrease the sampling rate by a integer number variable. A down-sampler with a down-sampling variable of M, where M is a positive number, fosters an output y[n] with a sampling rate that is $(1/M)^{th}$ of that of the input x[n] [17] - [20]. The down sampler is displayed in Figure1.

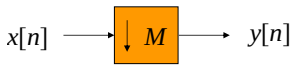

Figure 1. Down Sampler

Down-sampling activity is carried out by keeping each Mth sample of x[n] and eliminating M in the middle between samples to create y[n]. The input and output of down sampler can be communicated as:

$$y[n] = x[nM] \tag{2.1}$$

Applying the z-transform in above expression, the accompanying articulation happens:

$$Y(z) = \sum_{n=-\infty}^{\infty} x[Mn] z^{-n} \tag{2.2}$$

The articulation on the right-hand side of Equation (2.2) can't be straightforwardly communicated regarding X(z). To get around this issue, another succession x_{int} [n] can be communicated as:

$$x_{\text{int}}[n] = \begin{cases} x[n], & n = 0, \pm M, \pm 2M, \ldots \\ 0, & \text{otherwise} \end{cases} \tag{2.3}$$

Then

$$Y(z) = \sum_{n=-\infty}^{\infty} x[Mn] z^{-n} = \sum_{n=-\infty}^{\infty} x_{\text{int}}[Mn] z^{-n}$$

$$= \sum_{k=-\infty}^{\infty} x_{\text{int}}[k] z^{-k/M} = X_{\text{int}}(z^{1/M}) \tag{2.4}$$

Presently, x_{int} [n] can be formally connected with x[n] as follows:

$$x_{\text{int}}[n] = c[n] \cdot x[n] \tag{2.5}$$

Where

$$c[n] = \begin{cases} 1, & n = 0, \pm M, \pm 2M, \ldots \\ 0, & \text{otherwise} \end{cases} \tag{2.6}$$

A convenient portrayal of c[n] is given by:

$$c[n] = \frac{1}{M} \sum_{k=0}^{M-1} W_M^{kn} \tag{2.7}$$

Where

$$W_M = e^{-j2\pi/M} \tag{2.8}$$

Taking the z-transform of Eq. (2.5) and by utilizing Eq. (2.7), the following articulation happens:

$$X_{\text{int}}(z) = \frac{1}{M}\sum_{n=-\infty}^{\infty}\left(\sum_{k=0}^{M-1} W_M^{kn}\right)x[n]z^{-n} \tag{2.9}$$

$$\begin{aligned} &= \frac{1}{M}\sum_{k=0}^{M-1}\left(\sum_{n=-\infty}^{\infty} x[n]W_M^{kn}z^{-n}\right) \\ &= \frac{1}{M}\sum_{k=0}^{M-1} X\left(zW_M^{-k}\right) \end{aligned} \tag{2.10}$$

The spectrum of a factor-of-2 down-sampler with an input $x[n]$ is shown in Figure 2.

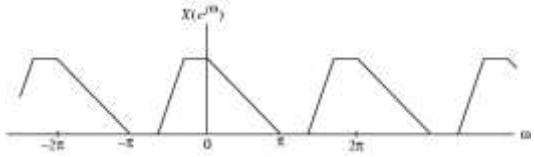

Figure 2. Down Sampler Spectrum

The DTFTs of the output and the input of this down-sampler are then related as:

$$Y(e^{j\omega}) = \frac{1}{2}\{X(e^{j\omega/2}) + X(-e^{j\omega/2})\} \tag{2.11}$$

The second term in above condition is basically acquired by moving the initial term X ($e^{j\omega/2}$) to right side by an amount 2π as displayed in Figure 3.

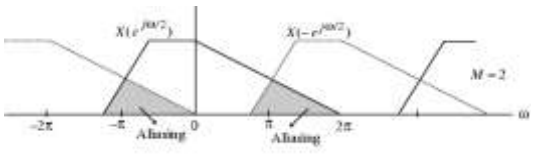

Figure 3. Aliasing Effect

The two terms have a cross-over because of which unique "shape" of X ($e^{j\omega/2}$) is lost when x[n] is down-sampled. This cross-over makes the aliasing that happens due to under-sampling. There is no cross-over, i.e., no associating, provided that:

$$X(e^{j\omega}) = 0 \qquad \text{for } |\omega| \geq \pi/2 \tag{2.12}$$

In general, Aliasing is absent if and only if:

$$X(e^{j\omega}) = 0 \quad for\ |\omega| \geq \pi/M \tag{2.13}$$

To conquer the impact of aliasing decimation filters are utilized. The specifications for the lowpass decimation filter are given by:

$$|H(e^{j\omega})| = \begin{cases} 1, & |\omega| \leq \omega_c/M \\ 0, & \pi/M \leq |\omega| \leq \pi \end{cases} \tag{2.14}$$

3. Design Modeling Simulation

The bandwidth of a signal is decreased to a proper worth during decimation so insignificant aliasing happens while decreasing the sampling rate. Multirate signal processing demands high performance decimator with less resources and computation requirements for cost effectiveness. A satisfactory transition width should be integrated into the design of the lowpass filter utilized for decimation alongside passband ripples and limited stopband attenuation. So, three decimators are designed and analyzed using 0.01 transition width, 0.01dB pass band ripples, 80dB stop band attenuation and decimation factor of 16 in Matlab environment [21].

Decimator 1

A multi-stage FIR decimator for above mentioned specifications has been designed and simulated for error analysis as shown in Figure 4. It can be analyzed from magnitude response of decimator 1 that the performance (Blue Plot) is well within the desired limits (Red Plot) but multiplier and adder requirement is more which in turn enhances the required computations.

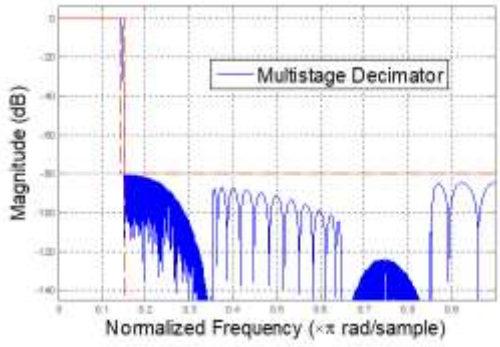

Figure 4. Decimator 1 Magnitude Response

Decimator 2

To fill the gaps of decimator 1, decimator 2 is designed and analyzed using multistage half band technique. Multistage half band decimator whose performance analysis is displayed in Figure 5. It can be observed from the decimator 2 magnitude response that it gives same stop band attenuation and transition width with a much lower order when contrasted with decimator1. The benefit of decimator 2 is less

multipliers and adder requirements which in turn reduces the computation. Lth-band filter with L = 2 is known as a half-band filter. The transfer function of a half-band filter can be communicated as:

$$H(z) = \alpha + z^{-1}E_1(z^2) \tag{3.1}$$

with its impulse response satisfying:

$$h[2n] = \begin{cases} \alpha, & n = 0 \\ 0, & \text{otherwise} \end{cases} \tag{3.2}$$

In Half band filters around half of the coefficients of h[n] are zero. It means that every alternative coefficient will zero and needs no computation. This decreases the quantity of multiplications and calculations expected in its implementation altogether. Decimator 2 output magnitude response (Blue Plot) is in desired limits (Red plot) but still resource consumption in terms of multipliers and adders needs attention.

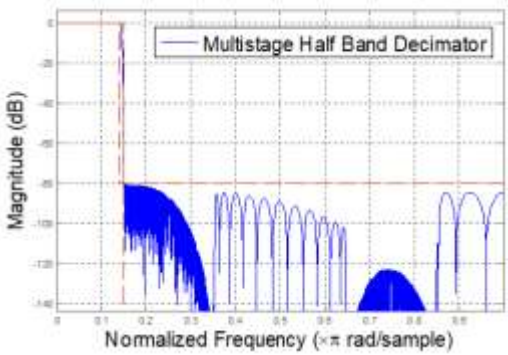

Figure 5. Decimator 2 Magnitude Response

Decimator 3

Decimator 3 is designed to further overcome the problems of decimator 2 using multistage Nyquist technique whose performance analysis is shown in Figure 6. It can be analyzed from Decimator 3 response that it is also meeting the desired specifications with significant reduction in multipliers, adders and computations.

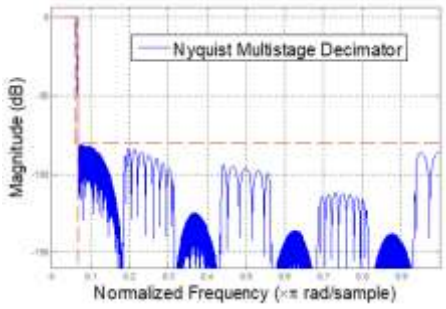

Figure 6. Decimator 3 Magnitude Response

4. Implementation Analysis

All decimators were synthesized and compared in terms of resources and computation requirements. All decimators were analyzed with respect to required multipliers, adders, MPIS and APIS. Decimator 1 requires 252 multipliers, 249 adders, 24.87 MPIS and 24.06 APIS. Its comparative analysis is shown in Figure 7.

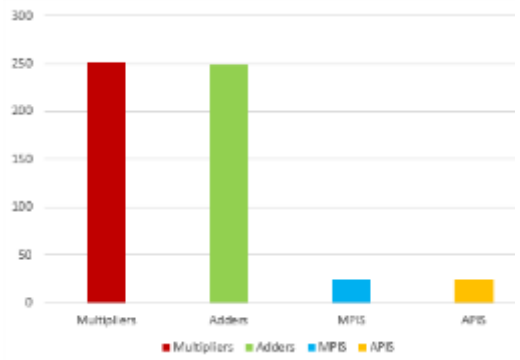

Figure 7. Implementation Analysis of Decimator 1

Decimator 2 implementation requires 235 multipliers, 232 adders, 20.37 MPIS and 19.56 APIS. Its comparative analysis has been shown in Figure 8.

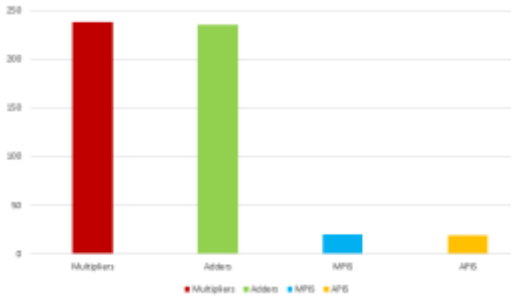

Figure 8. Implementation Analysis of Decimator 2

Decimator 3 implementation requires 84 multipliers, 80 adders, 9.4 MPIS and 8.5 APIS. Its comparative analysis has been shown in Figure 9.

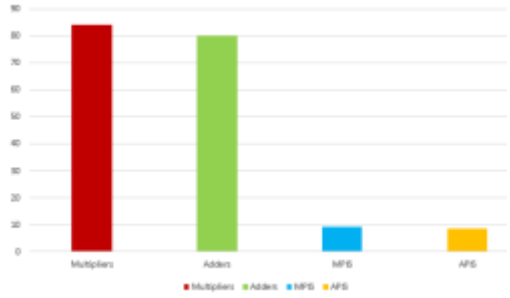

Figure 9. Implementation Analysis of Decimator 3

The comparative analysis of all the decimators is shown in Table 1 and its graphical comparative analysis is shown in Figure 10 respectively. It can be observed from the comparative analysis that the Decimator 3 shows significant reduction in required number of multipliers, adders, MPIS and APIS as compared to other two decimators.

Table1. Comparative Analysis

Design	Resource & Computation Comparison			
	Mult	Add	MPIS	APIS
Decimator 1	252	249	24.87	24.06
Decimator 2	235	232	20.37	19.56
Decimator 3	84	80	9.4	8.5

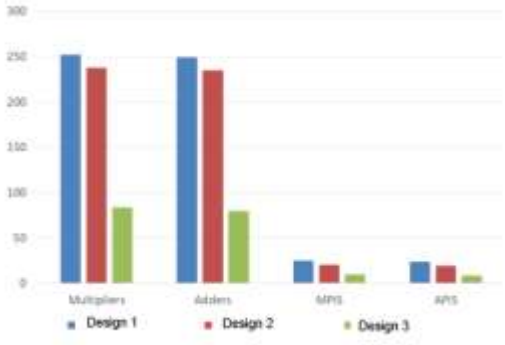

Figure 10. Implementation Comparison

The proposed decimator 3 reduces 64 - 67 % multipliers and 65 - 68 % adders as compared to decimator 2 and decimator 3. Decimator 3 also reduces 54 -62 % multiplications per input sample (MPIS) and 57 - 65 % additions per input sample (APIS) as compared to other two decimators.

5. Conclusions

In this paper, decimator is designed and analyzed utilizing three distinct procedures to reduce the resource and computation requirements. The simulated results show that performance of all the designs is according to wanted details however their resource and computation complexity varies significantly with regards to multipliers, adders, MPIS and APIS. The decimator 3 brings about decrease of 64 - 67 % multipliers and 65 - 68 % adders, for hardware implementation when contrasted with different decimators. So decimator 3 is best to perform down sampling and to give computationally successful solution for multirate signal processing applications.

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