Performance Evaluation of a Network-on-Chip Interconnect Architecture Based on Nanoelectronic Devices

EDYLARA RIBEIRO RANGEL[1] AND JANAINA GONÇALVES GUIMARÃES[2]
[1]Electrical Engineering Department, University of Brasília, P.O. Box 4386, CEP: 70919-970, Brasília – DF, Brazil
[2]Engineering Department, Federal University of Santa Catarina, Rua João Pessoa 2750, Blumenau – SC, Brazil
edylara.rangel@gmail.com, janaina.guimaraes@ufsc.br

Abstract: - In this work, a performance evaluation concerning energy consumption of a nanoelectronic Network-on-Chip (NoC) architecture considering interconnect effects will be presented. The goal is to determine the interconnection influence upon the NoC architecture, in a nanoelectronic system. For power consumption calculations it was used a nanoelectronic router based on single-electron transistors (SET). In this router the building block for designing all digital modules were a NAND gate. The mesh topology will be adopted, since most NoCs uses this network topology for regularity and modularity. Also, an analytic model for energy consumption in NoCs will be adopted. Finally, a short comparison between MOS and SET performances will be shown to reinforce the important role that nanoelectronic can offer for this type of architecture in the future.

Key-Words: - nanoelectronic, Network-on-Chip (NoC), interconnect, power consumption, carbon nanotubes (CNT), single-electron transistor (SET)

1 Introduction

Nanoelectronics appear to be the solution for continues scaling down circuits and to allow GSI (Giga-scale Integration) or TSI (Tera Scale Integration) implementations in the future [1]. Interconnection limits continue to be a problem in the evolution of integrated electronic circuits, especially in nanometric dimensions. Circuits based on nanoelectronic devices, such as single-electron transistors (SET), must take into account interconnection effects, since they have an important role in the total power dissipation and delay of the system [2]. Besides that, new technologies, like CNT are being studied to overcome limitations of copper interconnects in nanoelectronic circuits, such as electrical proprieties and eletromigration reliability.

Even in CMOS technology, one of the major problems comes from the advent of many-core architectures. Traditional dedicated bus-based communications are not capable to support the increasing requirements of future System-on-Chip (SoC). To tackle this bottleneck, Network-on-Chip (NoC) becomes a promising on-chip communication infrastructure, since this approach improves wire utilization and provides a highly structured and scalable solution.

Taking that into account, this paper evaluates the performance of a NoC architecture using nanoelectronic devices.

2 NoC Architecture

A NoC architecture system implementation consists of multiple intellectual property (IP) blocks, routers and links that are arranged in a specific topology depending on the application. The major part of NoCs design uses network topologies like mesh and folded torus for regularity and modularity [3]. Fig.1 shows the NoC architecture with mesh topology adopted in this work. The IP can be processors, memory elements, audio cores, etc. Each IP is connected to a local router through a Network Interface Controller (NIC). The NIC is responsible to packetize/de-packetize the data into/from the underlying interconnection network.

The router is the heart of the NoC system, responsible for transmitting the data from the source to its destination, based on several routing algorithms and control flow mechanisms. For a mesh topology, usually, a NoC router has five input ports and five output ports. For both inputs or outputs, four ports correspond to the four cardinal directions (North, East, South and West) and one to the local port, used for communication with the local IP [4], a crossbar switch which physically

links the input ports to its destined output ports, buffers and an arbiter that control the routing strategy and logical transfer data through the NoC. A typical 5-port router is illustrated in Fig.2.

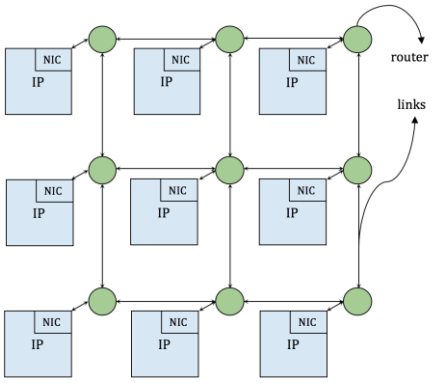

Figure 1. Network-on-chip architecture

In this work, the IPs are not represented because the goal is to evaluate the performance of a NoC interconnect architecture using nanoelectronic devices. The nanoeletronic router will be presented in the next section.

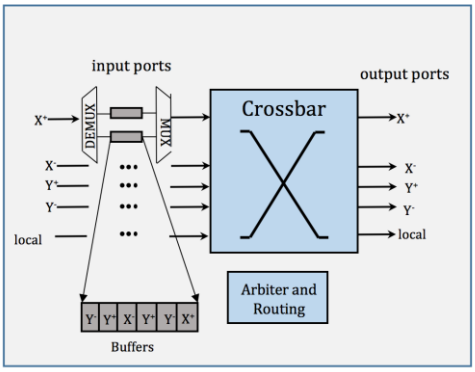

Figure 2. Typical 5-port router

3 Nanoelectronic router based on single-electron NAND gates

One simple nanoelectronic router architecture completely designed based on single-electron NAND gates has already been proposed [11]. The whole circuit diagram is shown in Fig. 3. The nanoelectronic router is composed by demultiplexers (DEMUX) and parallel-to-serial converters (PISO). Each input is forwarded accordingly to the look-up table given by the select lines of the DEMUX. The interconnection fabric is the direct connection between the input and output modules [11].

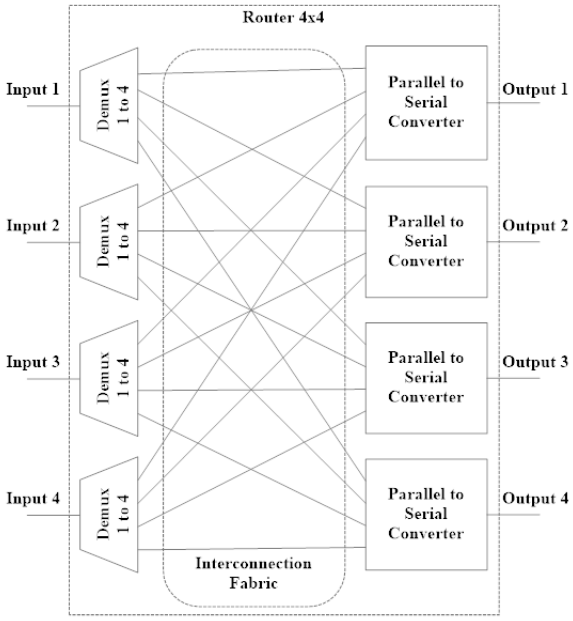

Figure 3. Nanoelectronic router diagram

In order to implement the simple nanoelectronic router 320 nanoelectronic NAND's were necessary. The SET model used for simulations was proposed by G. Lientsching *et. al* [7].

4 Simulation and results

Please, follow our instructions faithfully, otherwise you have to resubmit your full paper. This will enable us to maintain uniformity in the conference proceedings as well as in the post-conference luxurious books by WSEAS Press. Thank you for your cooperation and contribution. We are looking forward to seeing you at the Conference.

4.1 NoC architecture with interconnect effects

Copper interconnects are still the mostly used nowadays. [9,10]. Thereby, interconnects segments of copper were connected between the nanoelectronic routers. Inside the router interconnect effects were neglected. In simulations, several values of interconnect lengths were considered, for global local interconnection dimensions, since this type of interconnect is used in NoC architectures. . The π-model was used for analysing the copper interconnect behavior. Its circuit is shown in figure 4.

The traffic generation defines data transmission in a specific network, leading to the determination of origin and destination nodes as well as the message flow between them, which describes the communication and behavior of a settled application. The traffic generation definition and the routing algorithm allows the designer to evaluate de

network performance using the validation of application requirements.

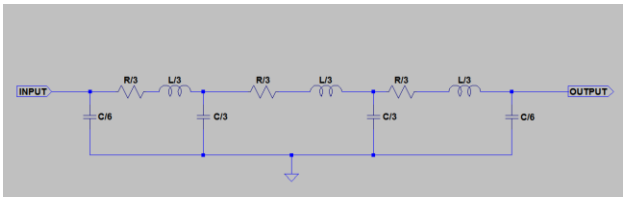

Figure 4. Copper interconnect π-model circuit

For spatial traffic distribution, some patterns are used to stress the communication architecture and its routing algorithm. In the random uniform traffic, each source has equal probability of sending packets to each destination. That traffic pattern is frequently used for evaluating a network because it is simple, makes no assumptions about the application and is analytically treatable. As the origin nodes do not distinguish if destination nodes are near or far, the random uniform traffic does not explore the communication locality and can be used as benchmark in non-ideal conditions.
The equation for obtaining the synthetic traffic CPD (Communication Probability Distribution) is given by equation (1), where Γ is the normalization coefficient which can be obtained by equation (2) and P(d) is probability of one wire connect two terminals separated by distance d.

$$CPD(d) = \Gamma P(d) * \sum_{i=1}^{2\sqrt{N}-2} \left(\sqrt{N} - i\right)\left(\sqrt{N} + i - d\right), \quad (1)$$

$$for\ 0 < \left(\sqrt{N} + i - d\right) \leq \sqrt{N}$$

$$\sum_{i=1}^{2\sqrt{N}-2} CPD(d) = 1 \quad (2)$$

Figure 5 shows the uniform random pattern CPD for a 8x8 mesh network.

4.2 Analytic model for energy consumption in NoCs

Analyzing the energy consumption of a NoC using simulations can be computationally expensive and forbidden, especially for systems with app oriented workload and in larger circuits. The analythical model proposed by Bezerra [12] was used in this work for evaluating the power consumption of NoCs based on nanoelectronic devices. That model was developed for direct networks which have the same length between nodes, i.e., all hops are equal, as, for example, in mesh or toroid networks.

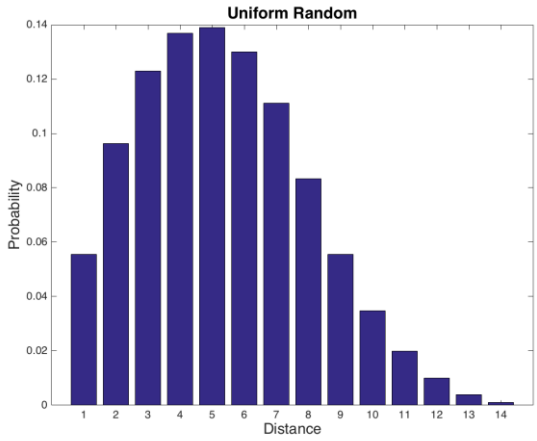

Figure 5. CPD for uniform random traffic pattern in a 8x8 mesh network.

The average energy per flit to travel a path with length d in a NoC is given by equation (3), where E_link and E_router are the energy consumed by the flit to go through a link and a router, respectively, and d is the number of hops traveled in the flit transmission from the origin node to the destination node [12].

$$E_{flit}(d) = d \cdot E_{link} + (d+1) \cdot E_{router} \quad (3)$$

The total energy consumed by a NoC, which represents the communication between the nodes of an application, is obtained by equation (4). So, the total energy consumed is given by the sum of the average energy per flit over all communication distances which connect nodes inside a determined network topology weighted by the probability of a packet travel that distance. That value is multiplied by the number of flits per packet (N_flits) and the total number of packets (N_packets). In equation (4) it is assumed that the number of flits per packet is constant [12].

$$E_{total} = N_{packets} \cdot N_{flits} \cdot \sum_{d=1}^{max} E_{flit}(d) \cdot CPD(d) \quad (4)$$

The total energy of the link was obtained from simulations. For all nodes presented, the energy consumption of a 1mm length interconnection is of approximately 113fJ/bit.

4.3 NoC architecture power consumption

Based on the nanoelectronic router circuit proposed by Câmara [11] it was possible to estimate the power value of that router for various flit sizes. For comparison, a 64-bit flit was used. In this case, the nanoelectronic router will consume approximately 7.68 pJ while the total link consumption will be 7.2 pJ. Finally, to calculate the whole NoC energy for

the specified traffic pattern, 20000 packets were injected in the network where k. Each packet has 5 flits. Owing to E_link and E_router values are similar for all technology nodes presented, the energy consumption of different mesh NoC sizes operating in 1 GHz is shown in figure 6 considering MOS routers NoCs and nanoelectronic routers NoCs. As can be seen, the router consumes the most part of the energy in a communication architecture, since the in both cases copper interconnects were used. In this way, using nanoelectronic devices is a promising alternative for reducing the total energy consumption.

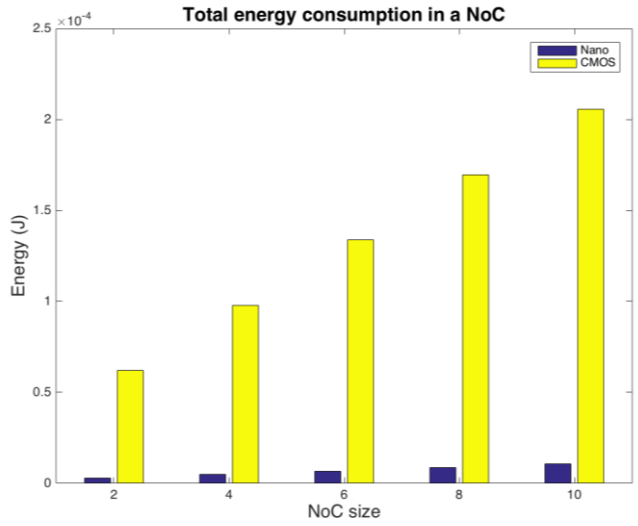

Figure 6. Performance comparison between MOS and nanoelectronic NoCs

5 Conclusions

In this work, the performance evaluation of a NoC interconnected architecture using nanoelectronic devices was proposed and its energy was estimated. This works shows the potencial of using nanoelectronic devices for NoC architectures. With the reduce of the devices, the energy dissipated in a system is becoming a huge problem. Thereby, the gain introduced by nanodevices is very promising and can provide a substantial reduction in the total energy of the system.

Acknowledgements

The authors are grateful to PQ/CNPq and INCT-NAMITEC for support.

References:

[1] J.A. Davis, R. Venkatesan, A. Kaloyeros, M. Bylansky, S.J. Souri, K. Banerjee, K.C. Saraswat, A. Rahman, R. Reif, and J.D. Meindl, "Interconnect Limits on Gigascale Integration (GSI) in the 21st Century," Proceedings of the IEEE, vol. 89, no. 3, pp. 305-324, March 2001.

[2] J. G. Guimarães and J. C. da Costa, "Interconnect Impact on the Performance of a SET-Based Network-On-Chip Memory Circuit" 14th IEEE International Conference on Nanotechnology, 2014, Toronto, vol. 1, pp. 287-290.

[3] M. M. Wanjari, P. Agrawal and R. V. Kshirsagar, "Design of NoC Router Architecture using VHDL", International Journal of Computer Applications 115(4), pp.18-21, April 2015.

[4] C. A. Nicopoulos, " Network-on-chip architectures: a holistic design exploration", Ph.D. Thesis, Department of Electrical Engineering, Pennsylvania State University, 2007 .

[5] S. Park, M. Qazi, L.S. Peh and A.P. Chandrakasan, "40.4 fJ/bit/mm low-swing on-chip signaling with self-resetting logic repeaters embedded within a mesh NoC in 45 nm SOI CMOS", Proceedings of Design Automation and Test in Europe (DATE), March 18–22, Grenoble, France, 2013.

[6] M. O. Telles and J. G. Guimarães, "Single-electron shift register", Microelectronics Journal, vol.44, 332 (2013).

[7] G. Lientshnig, I. Weymann, P. Hadley, "Simulating hybrid circuits of single-electron transistors and fiel-effect transistors", Jpn J. Appl. Phys., vol. 42, no. 10, pp. 6467-6472 (2003)

[8] Linear Technology – Design Simulation and Device Models Retrieved, December, 2015, from http://www.linear.com/designtools/software

[9] N. Srivastava, H. Li, F. Kreupl, K. Banerjee, "On the applicability of single-walled carbon nanotubes as VLSI interconnects", IEEE Transactions on Nanotechnology, vol. 8, no. 4, pp. 542-558

[10] C. Thiruvenkatesan, J. Raja, "Studies on the application of carbon nanotube as interconnects for nanometric VLSI circuits", ICETET'09, pp. 162-167.

[11] B. O.. Câmara, J. G. Guimarães and J. C. da Costa, "Proposal of a router circuit based on nanoelectronic devices" TechConnect Briefs 2016 - Advanced Manufacturing, Electronics and Microsystems, 2016, Washington, vol. 1, pp. 183 – 187, May 2016

[12] G. B. Bezerra, "Energy consumption in networks on chip: efficiency and scaling", PhD Theses, The University of New Mexico, 2012.